Teaching Comprehensive Real-World VLSI Design to Undergraduate Students

Orlando J. Hernandez
E-mail: hernande@tcnj.edu
Department Electrical & Computer Engineering
The College of New Jersey
Ewing, New Jersey 08628-0718, USA

ABSTRACT

This paper presents a case study on the challenges of teaching state-of-the-art design to undergraduate students with projects that emulate those encountered in any given company developing commercial semiconductor technology and products. The issues encountered are exposed specifically through the discussion of the development and teaching of a comprehensive first course in Very Large Scale Integrated Circuit (VLSI) design at The College of New Jersey (TCNJ).

Keywords: Design Education, Undergraduate Education, Undergraduate Practice, VLSI Design

1. INTRODUCTION

Microsystems and Information Technology is one of the largest industries, approximating $1.2 Trillion currently, and is expected to grow to $3.0 Trillion within a decade. Two critical items, however, must be addressed before this growth can become a reality. First, new technologies are needed both to create new products and to expand the existing products based on the last 40 years of the microelectronic revolution. These new technologies must lead to marketable products that are higher in performance, lower in cost, thin, light, portable, and highly reliable. Second, new human resources trained in these new technologies and products must also be developed to propel the market growth. These engineers are needed to explore, design, develop, manufacture and market the products globally [1]. As these new technologies are developed, educational institutions still have the responsibility to equip students with a well-balanced education. This balance must consist of a solid coverage of the fundamentals, and additionally, a coverage and perspective of these new technologies, as they relate the industrial environment in which students will be operating after graduation. Graduates will be expected to use these new technologies, and ultimately improve upon them as they join the workforce as productive members of society. Achieving this balance is a challenge faced by all academicians, but it is more pronounced for those in fast evolving fields that are highly technological in nature. Such a field or technology is the development of state-of-the-art semiconductor or microelectronic products, or VLSI design.

VLSI design is a fast paced field that deals with many advanced technologies, and the experiences and issues encountered during the development and teaching of a comprehensive and intensive first course in VLSI design course can be useful not only to the Electrical and Computer Engineering teaching community, but to all Engineering teachers at large. Some of the issues encountered are the level of preparation or pre-requisite knowledge that the students must have so that the model is successful; the reaction of students to modern and very specialized Computer Aided Design (CAD) tools; how students deal with uncertainty, lack of data, and degrees of freedom encountered during design activities; and the reaction of student to the intensity of such a course from the perspectives of breath, depth, and level of difficulty of assignments that mirror those that can be expected to be received in the workplace.

1.1 Some Recent Related Activities and Studies

An introductory VLSI Design course for undergraduate students was developed at Harvey Mudd College to reconcile the tension faced by such courses between teaching good design practices by example and giving students the freedom to learn for themselves through open-ended team design projects [2]. On one hand, guiding students through implementation of a well-planned chip is an efficient way to teach design and verification methods, CAD flow, and proper use of data-paths, arrays, and synthesized logic. On the other hand, permitting students to select and carry out a design project of their own choice through tape-out is very motivational and provides a deeper mastery.

The University of Michigan has been at the forefront of VLSI education for years, and an introductory VLSI Design course has been taught there since 1980. In 1990, it was redesigned around a simple 8-bit microprocessor project, and in 1996, the project was updated to a 16-bit Reduced Instruction Set Computer (RISC) processor. [3] describes the course philosophy,

content, and the baseline architecture from which class projects begin. The key features of the course are: close coordination of lectures and project activity; prompt and regular feedback on design work; and a schedule which spreads the workload over the full term. In this course, students learn VLSI fundamentals and good design methodology that will be important throughout their careers.

The work described in [4] presents a novel approach to teach computer organization concepts with extensive hands-on design experience very early in Computer Science curricula. While describing the proposed teaching method, it addresses relevant questions about teaching VLSI design to students in computer science and related fields. The approach involves the analysis, simulation, design and effective construction of processors. It is enabled by the use of both, VLSI hardware prototyping platforms constructed with re-configurable hardware and powerful computer aided design tools for design entry, validation and implementation. The approach comprises a 4-hour a week lecture course on computer organization and a 2-hour a week laboratory, both taught in the 3rd semester. In the first two editions of the course, most students obtained successful processor implementations.

In [5], a VLSI design course involving a team of 4 professors and 6 associate professors is proposed at the undergraduate level. There would be 70 engineers trained in VLSI design each year and there would be 250 hours of lectures and 30 hours of experimental work. This training is completed by an IC test course (30 hours) on the basics of fault modeling, fault simulation and test generation, which includes advanced concepts such as Design for Test (DFT), Built-In Self Test (BIST), delay test, current test and analog test.

2. COURSE OUTLINE

The VLSI Design course at TCNJ has four hours of lecture per week, and attempts to comprehensively cover structured design methodologies for VLSI systems. The lecture part of the course is complemented by a mid-term test and a non-comprehensive final test. The choice of making the final test non-comprehensive is a conscious one, so that the students focus more on their third and largest hands-on design project that must be completed before the end of the semester as described later. Homework is also assigned from all chapters of the text, collected, and graded. The grading policy places 10% weight on the homework, 25% on each test, and 40% on the three projects that will be described in the next section. These are weighted as follows: Project 1 = 10%, Project 2 = 10%, and Project 3 = 20%. Topics of the course include switching models, device equations, combinational, sequential, and analog systems design, simulation, timing, verification, and tools for computer-aided design. The course does not attempt to spend any time given a broad initial overview of all the topics to be covered during the whole semester, but instead immerses the students into the details following a bottoms-up approach from a technology perspective. The texts used in the course are the classic VLSI Design book by Weste and Eshraghian [7], along with its companion book on Hardware Description Languages (HDLs) [8]. The course is structured as follows.

CMOS PROCESS TECHNOLOGY

This first section of the course introduces the bulk Complementary Metal Oxide Silicon (CMOS) process technology exclusively focusing on it with a fair amount of depth, while not spending any time on other technologies like Bipolar or Silicon on insulators. The CMOS process is by far the most widely used VLSI technology. The level of depth helps the students understand the limitations of the technology.

The basics of semiconductor manufacturing are first introduced. Following this, basic n-well, p-well, and twin-tub CMOS processes are described, including the enhancements necessary to make the technology analog friendly, and that are necessary to take advantage of the large amounts of functionality integration possible with today's and future geometries.

Together with the description of the process steps, layout rules are discussed. These, along with the electrical extraction rules that are discussed in a subsequent part of the course, form the link between the designer and the manufacturing engineer. Finally, process specific reliability issues like latch-up are also discussed during this part of the course.

For developing the appropriate workforce of the 21st century for the semiconductor industry, detailed knowledge must be acquired by students not only in design, but also in mask fabrication and wafer processing technologies [9].

MOS TRANSISTOR THEORY

This section examines the characteristics of CMOS transistors in detail to lay the foundation for predicting the performance of the devices. The section focuses on both DC and AC characteristics, and it encourages the students to achieve proficiency at being able to calculate circuit performance by hand and intuitively at a first order of approximation only. Any detailed circuit behavior is acquired by detailed computer simulation with SPICE.

CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION

This section exposes the student to simple models that assist the understanding of system behavior, and that provide the basis whereby systems performance, in terms of signal delays and power dissipation, can be estimated. Issues considered in this section are resistance, capacitance, and inductance calculations and rules for automated computer based extraction; delay estimation; determination of conductor size for power and clock distribution; power consumption; design margining; reliability; and effects of scaling.
Much emphasis is made on the fact that robust characterization methodologies are fundamental to successful VLSI design systems, and that these must be comprehensive and therefore automated by the aid of computers and extraction and simulation software.
The timely issues of increasing interconnect contribution to digital CMOS circuit delays and power is covered at length. Since interconnect is becoming a limiting constraint for microelectronics technology, VLSI design curricula require the introduction of interconnect performance into VLSI design classes [10].

CMOS CIRCUIT AND LOGIC DESIGN
This section treats in detail the fully complementary style of design for CMOS logic gates. Better than 95% of all designs in CMOS can be implemented with a complementary style and it delivers a very attractive performance/power ratio with very little complexity. This makes focusing on this style ideal for a first course in VLSI Design that attempts to cover many other issues comprehensively. Clocking strategies, storage, non-ideal switching circuit behavior, and I/O circuits are also treated in this section.
The structured approach to VLSI design is also introduced in this section. Circuit and layout design flows are described, and treated concurrently, as these two phases of the design cycle are intimately meshed.
Packaging issues are also introduced, which is a key component to the comprehensive understanding of VLSI technology [1].

CMOS DESIGN METHODS
This section focuses on chip level design flows, and the students acquire a level of understanding to be able to draw a diagram of a whole VLSI design flow/system from circuit to chip. Design concepts like regularity, modularity, and abstraction are covered, and design descriptions are discussed, and how these descriptions are implemented at different levels of abstraction. Some points of design economics and good design documentation practices are also covered.
The power of EDA tools is emphasized in this part of the course [6]. The increasing complexity of VLSI systems has led to the development of sophisticated CAD tools that use HDLs to describe hardware designs at various levels. Based on the recent industry shifts, it has become clear that HDLs have become an integral part of design automation environments. This has created a demand for future engineers that are well trained in HDL-based design methodologies [11]. In our course, an HDL is introduced in this section. The course is agnostic with respect to which HDL to teach. Both Verilog® and VHDL are equally used in the industry, and therefore the goal of the academic program is to teach Verilog®, which is easier for students to grasp, in the lower level Digital Circuits and Microprocessors course, and VHDL in VLSI Design. However; when it is time to cover the HDL for the VLSI Design course, a poll is taken, and if most students have not been exposed to Verilog®, then this is the HDL taught, instead of VHDL.
In light of the relationship between CAD tools and design complexity, a great deal of time is spend in this section of the course discussing Application Specific Integrated Circuits (ASIC) design methodologies, Systems-on-a-Chip (SoCs), and system level design. Deep-Sub-micron (DS) CMOS technology is rapidly enabling the integration of processors, memory, mixed-signal (digital and analog), and even RF architectures. In today's electronic products, almost any gadget can be abstracted in such a way, so that it can be implemented as a single integrated chip containing these components: Processor, memory, data conversion, power electronics, and radio circuits. However, exploitation of DS technology will depend critically on the availability of global system engineers able to bridge the gap between software-centric system thinking and hardware-software implementation in novel silicon architectures [12]. Therefore, VLSI education needs to continually emphasize system issues and associated physical constraints [13].

CMOS TESTING
This section covers how CMOS chips are tested at different levels and stages of the manufacturing process. Fault models, test types (scan and Automated Test Pattern Generation - ATPG, BIST, delay test, IDDQ, analog), test planning and partitioning, and test economics are also covered. It is emphasized that Design for Test (DFT) is much of a design issue, and therefore the development of feasible and economically sound test strategies is essential for product success [14], [5], [15].

CMOS SUBSYSTEM AND SYSTEM DESIGN EXAMPLES
This section goes through the details and examples of CMOS subsystem design. Emphasis is on data-path operators, memory elements, control structures, and

more details on I/O cells that had been previously covered in the course.

During this part, students engage with the instructor in deep discussions about design partitioning and tradeoffs, such as speed/performance, density and cost of build (COB), programmability, ease of design which is related to time to market for any given product, and many other variables. These are specifically important concepts for students to grasp, and they get first hand experience at how design decisions are made without having all the variables known at time zero. Although students tend to have a difficult time with this reality, it is one that needs to be introduced as soon as possible in engineering curricula, so that students start getting comfortable with it, and finish adapting when they enter the work force. The alternative of shocking new engineers into the fuzzy decision process of real world design short-changes prospective employers. The concept of step-wise refinement and iterations through the design process is also reinforced. Students gain a strong appreciation for what different levels of design hierarchy are, and how they are related from a design and Intellectual Property (IP) reuse perspective, as they understand that that these subsystems can be used to design systems (chips, chip sets, or boards) of considerable complexity.

At this point, specific efforts are taken to introduce students to subsystems of a mixed signal nature, such as Phase-Locked Loops (PLLs) and a 6-bit Flash Analog to digital Converter (ADC).

ANALOG VLSI DESIGN INTRODUCTION

As the lecture material for the course winds down, students are introduced in this last part to the details of several CMOS implementations of several analog circuits: current mirrors, differential amplifiers, and simple voltage regulators.

The techniques used to craft specific devices like capacitor and diodes that are not necessarily used in digital logic are also covered. This also includes layout techniques that are specific to analog CMOS VLSI, such as common centroid layout.

This section cues form the mixed signal examples offered in the previous on, and gives student a window into what a second course in VLSI design would be like, which should be focused on analog VLSI technology.

3. PROJECTS

To strongly complement the intensity offered by the lecture side of the course in terms of breath and depths of the CMOS VLSI design field, three projects are scheduled through the semester. These projects resemble small projects that an entry level design engineer may be assigned at a semiconductor company. These are to be completed by the students in an individual basis, and students are expected to spend considerable non-scheduled class time in these projects. The tools used for the transistor level design projects (Projects 1 and 2) are the suite of tools for IC design from Mentor Graphics Corporation (MGC) as expanded in Table 1. For Project 3, where students get to design a module using an HDL, the Xilinx programmable logic design environment with the MGC ModelSim simulator is used. The MGC IC design tools run on a Linux server that students access from PCs running an X-Windows emulation program, and the Xilinx tools run natively on the PC platform.

It is important to highlight that the VLSI Design Laboratory is large enough to accommodate every single student in the class, and that appropriate tutorials of the tools are taught by the instructor before the use of the tools is required in the course. Details of the projects follow.

Table 1. IC Design Tool Suite

TOOL	FUNCTION
Design Architech	Circuit schematic capture, netlisting, transistor level simulation setup, and results viewing
IC Station SDL	Polygon editing, hierarchical, schematic and netlist driven layout, and parameterized device generator
Calibre	Physical verification, manufacturability, and resolution enhancement
Calibre xRC	Parasitic extraction
Eldo	Classical (Newton-Raphson) and advanced (OSR and IEM) algorithms for SPICE-level simulation and analysis

PROJECT 1:
DESIGN OF A COMPLEX GATE

In this project, a complex gate is designed. There are two parts to the project. First, a standard load (SL) is designed. The next step is the design of the complex gate, then the layout. A report is to be submitted by each student by the due date informed during class. Each student is expected to do all work individually. All reports are written in a word processor and similar productivity computer tools; no hand written reports are accepted. Projects 2 and 3 also have the same ground rule requirements.

For the design of the SL, students design an inverter that is used as a standard load in a characterization procedure in Project 2. This inverter shall utilize a minimum size n-transistor, and the appropriate

minimum size p-transistor to achieve within 10% equal rise and fall times and/or propagation delays without any load and using the slow transistors parameters. First, students are instructed to layout an n and a p transistor in to find out what are the minimum transistor sizes. Then they capture and simulate the inverter with 0.1 nS input edges. Then, calculate the input capacitance of the inverter. Subsequently, they make a symbol and a SPICE sub-circuit for this inverter.

For the complex gate, students design, simulate, and layout a logic gate to perform the following function:

$$f = \overline{A\,(B + C\,D\,E)} \qquad (1)$$

Through this project, students get practical experience on how to match design to specifications via first order calculations as a starting point, and then iteratively refining the design based on feedback from detailed computer based simulations. The concept of design corners (process, temperature, and supply voltage) is also reinforced through this project. This is a very important concept in real world VLSI design.

PROJECT 2:
DESIGN AND CHARACTERIZATION OF A FLIP-FLOP

In this project, a flip-flop is designed and characterized. There are two parts to the project. First, the flip-fop is designed and laid out. Then, the module is characterized as well.

Students design a D flip-flop that is positive edge triggered, with Q output, and with active low clear input as well. The load to be considered for the design of the flip-flop is 2 SL from Project 1. They are instructed to design the flip-flop using the same transistor sizes that were used for the standard load in Project 1. This applies to all the transistors in the flip-flop, except for the ones making up the output driver stage. These are to be sized per the load discussed above, so that both output rise and fall times are less than 1 nS. The design is captured, and students make sure through simulation that it meets the output strength spec. 0.1 nS input edges are used. The additional specs for this flip-flop are that the hold time is 0 nS or negative. Notice that to reinforce the point of specs not being an exact number or some times not given, a one sided spec is given for the hold time, and no spec is given for the setup time. The simulations are done with the slowest corner for the output strength and the fastest corner for the hold time. Students are also required to make a symbol and a SPICE sub-circuit for this flip-flop.

After the first version of the flip-flop is designed, students layout, back-annotate parasitic capacitances, and re-simulate to check that specs are still being met. If the specs are not met, the design and the layout are refined iteratively, so that the specs are met and the schematic and the layout are coherent.

At this point, there is a fully designed and laid out circuit that meets both functional and performance requirements. Then the flip-flop must be characterized. The following parameters are characterized: propagation delay from clock to Q with the output switching low to high (t_{CQLH}), propagation delay from clock to Q with the output switching high to low (t_{CQHL}), setup time (t_{SU}), rise and fall times of the output, and propagation delay from reset to Q (t_{RQ}). The characterization is to be done at this process, voltage, and temperature (PVT) corner with all the combinations of the following loads and input slews:

- Slow corner: slow n-channel SPICE model, slow p-channel SPICE model, low voltage, and high temperature.
- Loads: 2 SL, 8 SL
- Slews (10% to 90%): 0.2 nS, 4nS

This characterization will yield one 2 x 2 table for each of the parameters.

Next, the following parameter is characterized: hold time (t_{HO}). The characterization is to be done at this process, voltage, and temperature (PVT) corner with all the combinations of the following loads and slews:

- Fast corner: fast n-channel SPICE model, fast p-channel SPICE model, high voltage, and low temperature.
- Loads: 2 SL, 8 SL
- Slews (10% to 90%): 0.2 nS, 4nS

These characterization will yield one 2 x 2 table.

Students are also to simulate the results of the supply current for two cycles of operation with all nominal transistors parameters, 5V V_{DD}, 25 ^{O}C, 2 nS 10-90% input slews, and 4 SL at the output.

While continuing the skill building trend started with Project 1, this project reinforces the concept of extensive characterization via circuit simulation, and since the characterization exercise tends to be long and tedious work, the importance of automation whenever possible in design is brought to light. Therefore, students are strongly advised to automate the characterization task via a Tool Control Language (TCL).

PROJECT 3:
DESIGN, VERIFICATION, IMPLEMENTATION, AND VALIDATION OF A BOUNDARY SCAN TAP CONTROLLER

In this project, a Boundary Scan Test Access Port (TAP) controller is designed, verified, implemented in Field Programmable Gate Array (FPGA), and validated. As such, there are four parts to this project.

After the module is designed, students write an HDL (Verilog® or VHDL) test bench to simulate and verify the controller, by having it follow and visit all the states of the Algorithmic State Machine (ASM) chart provided as part of the specification for the controller.
The design is implemented in the Xilinx FPGA board with a timing constraint to make the design run as fast as possible (50 MHz max), and a timing analysis is performed. Finally, the design is validated once implemented in the FPGA board repeating the steps of the verification test bench, but this time directly on the FPGA, and the results are captured.
This project attempts to highlight and summarize together concepts related to chip design, such as verification, implementation, functionality, performance and timing, and validation once a prototype is available.

4. CONCLUSIONS

This paper describes a comprehensive first course in VLSI design at TCNJ. This course attempts to provide a solid foundation in VLSI design with an amount of detail and practice that will enable students to productively do design, and a breath of the subject matter that spans silicon process technology, digital and analog design, as well as system issues. The goal is to provide student with powerful learning experiences that they can easily transfer to a future workplace.

5. REFERENCES

[1] R. Tummala and L. Y. Conrad, Undergraduate Microsystems Packaging Education: Needs, Status and Challenges, Proceedings - Electronic Components and Technology Conference, 2001, pp. 1276-1281.

[2] D. Harris, The Microprocessor as a Microcosm: A Hands-On Approach to VLSI Design Education, Proceedings - Frontiers in Education Conference, vol. 3, 2002, pp. S2D/1-S2D/5.

[3] R. B. Brown, B. Richard, R. J. Lomax, G. Carichner, A. J. Drake, Microprocessor Design Project in an Introductory VLSI Course, IEEE Transactions on Education, vol. 43, no. 3, 2000, pp. 353-361.

[4] N. L. V. Calazans, F. G. Moraes, VLSI Hardware Design by Computer Science Students: How Early Can They Start? How Far Can They Go?, Proceedings - Frontiers in Education Conference, vol. 3, 1999, pp. 13c6-12 - 13c6-17.

[5] M. Robert, Increasing Test Coverage in a VLSI Design Course, Proceedings of the 1999 ITC International Test Conference (ITC'99), 1999, p. 1135.

[6] L. T. Walczowski, K. R. Dimond, W. A. J. Waller, Digital Engineering Curriculum with Integrated, Windows-Based EDA Tools, Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems, vol. 3, 1998, pp. 425-428.

[7] N. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, Second Edition, Addison-Wesley, 1994.

[8] M. J. S. Smith, Excerpts of Chapters 10 & 11 from Application-Specific Integrated Circuits: An Introduction to VHDL & Verilog HDL, Addison-Wesley, 2001.

[9] K. Prasad, Preparing the Workforce for Semiconductor/VLSI Industry for the 21st Century at UMASS Lowell, Proceedings of the 2000 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 2000, p. 193.

[10] R. Mangaser and K. Rose, Facilitating Interconnect-Based VLSI Design, Proceedings of the 1997 IEEE International Conference on Microelectronic Systems Education, MSE'97, 1997, pp. 139-140.

[11] A. Sagahyroon, On the Use of Hardware Description Languages in Teaching VLSI Design Courses, Proceedings - Frontiers in Education Conference, vol. 2, 1996, pp. 713-716.

[12] H. De Man, Future Systems-on-a-Chip: Impact on Engineering Education, Proceedings of the IEEE International Conference on VLSI Design, 1998, pp. 572-577.

[13] L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen, System Oriented VLSI Curriculum at KTH, Proceedings of the 1997 IEEE International Conference on Microelectronic Systems Education, MSE'97, 1997, pp. 57-59.

[14] G. Russell, Teaching of “Design for Test” – Mythconceptions, Proceedings of the 1998 IEE Colloquium on the Teaching of Digital Systems, no. 409, 1998.

[15] M. L. Bushnell, Increasing Test Coverage in a VLSI Design Course, Proceedings of the 1999 ITC International Test Conference (ITC'99), 1999, p. 1133.

About the Author – Orlando J. Hernandez received his Ph.D. degree in Electrical Engineering from Southern Methodist University in 2002. He is currently an Assistant Professor of Electrical & Computer Engineering at The College of New Jersey, Ewing, New Jersey. His research interests include computer vision, image processing, and computer architecture. Before joining TCNJ, he spent ten years in the industry at Texas Instruments Inc. and Maxim Integrated Product Inc. where he held positions in Product Development, Design Management, and Business Management.