

**ENG 312**  
**DIGITAL CIRCUITS AND MICROPROCESSORS**  
**(3 lecture hours, 1 design hour)**

**Course Information**

**Professor: Orlando Hernandez**

**Spring 2013: MW 5:30PM–6:50PM/6:55PM-7:20PM/AR148**

**Course Description:** Analysis and design of digital systems including Boolean algebra, combinational and sequential circuit design, programmable logic devices, HDL, CMOS logic circuits and computer basics.

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**Office Hours:** Tuesdays 4:00 PM - 5:20 PM  
Thursdays 10:00 AM - 11:20 AM  
By appointment (send me email)  
And whenever my office door is open

**Textbook:** *Digital Design*, Fifth Edition, by M. Morris Mano and Michael D. Ciletti, PEARSON Prentice Hall, 2013.  
ISBN-13: 978-0-13-277420-8 ISBN-10: 0-13-277420-8

**Corequisite:** Computer Science I for Science and Engineering (CSC 215) or permission of the instructor

**Grading Policy:**

Homework	10%
Homework will be announced for each chapter after the chapter has been covered.	
Four Tests	40% (10% each)
Comprehensive Final Exam	30%
Design Projects	20% (Projects 1 and 2: 5% each, Project 3: 10%)

**Tips for Success:** Read the book sections prior to their discussion in class.  
Do as much homework as possible. Attempt to do all the problems, even the ones that have not been assigned.  
Do not be shy about asking questions, either during class or outside of the class.

**College Level Policies:** Attendance Policy: <http://www.tcnj.edu/~recreg/policies/attendance.html>  
Academic Integrity Policy: <http://www.tcnj.edu/~academic/policy/integrity.html>  
Americans with Disabilities Act (ADA) Policy: <http://www.tcnj.edu/~affirm/ada.html>

**Tentative Agenda:**

Week	Topics	Reading
1, 2	<b>DIGITAL SYSTEMS CONCEPTS</b>	
Monday 1/21	Data Representation	CHAPTER 1.1 – 1.9
Monday 1/28	Binary and Decimal Numbers	
	Cells and Hierarchy	
	<b>PROJECT ORIENTATION AND LECTURE</b>	

**Tentative Agenda (continued):**

Week	Topics	Reading
3 Monday 2/4	<b>BOOLEAN ALGEBRA AND LOGIC GATES</b> Logic Operations and Identities AND and OR gates Canonical Logic Forms Logic NAND and NOR Sets <b>PROJECT 1: INTRODUCTION TO XILINX</b>	CHAPTER 2.1 – 2.8
4, 5, 6 Monday 2/11 Monday 2/18 Monday 2/25	<b>TEST #1</b> <b>GATE-LEVEL MINIMIZATION</b> Algebraic Reduction Karnaugh Maps NAND and NOR Implementation Digital Hardware Considerations Exclusive-OR <b>HDL BASICS</b> <b>PROJECT 1: INTRODUCTION TO XILINX</b>	CHAPTER 3.1 – 3.9
7, 8, 9 Monday 3/4 Monday 3/11 Monday 3/18	<b>COMBINATIONAL LOGIC COMPONENTS</b> Equality and BCD Detectors Line Decoders Multiplexers and Demultiplexers Binary Adders Subtraction and Multiplication <b>PROJECT 2: COMBINATIONAL LOGIC DESIGN</b>	CHAPTER 4.1 – 4.11
10, 11 Monday 3/25 Monday 4/1	<b>TEST #2</b> <b>SYNCHRONOUS SEQUENTIAL LOGIC NETWORKS</b> Sequential Network Concepts Latches, Clocks and Synchronization Flip-Flops Sequential Network Design <b>PROJECT 2: COMBINATIONAL LOGIC DESIGN</b>	CHAPTER 5.1 – 5.7
12 Monday 4/8	<b>REGISTERS AND COUNTERS</b> Registers Counters <b>PROJECT 2: COMBINATIONAL LOGIC DESIGN</b>	CHAPTER 6.1 – 6.6
13 Monday 4/15	<b>TEST #3</b> <b>MEMORY ELEMENTS AND ARRAYS</b> RAM, ROM and CD ROM Memory Decoding Error Detection and Correction ROM, PAL, PLD Implementations <b>PROJECT 2: COMBINATIONAL LOGIC DESIGN</b>	CHAPTER 7.1 – 7.8
14, 15 Monday 4/22 Monday 4/29	<b>REGISTER TRANSFERS</b> Register Transfer Level ASMs Control Logic <b>PROJECT 3: SEQUENTIAL LOGIC DESIGN</b> <b>TEST #4</b>	CHAPTER 8.1 – 8.9
16 Monday 5/6	<b>COMPREHENSIVE FINAL EXAM</b>	

## **Educational Objectives**

*(What TCNJ ECE engineers should be able to accomplish during the first few years after graduation)*

The Department of Electrical and Computer Engineering at the College of New Jersey seeks to prepare its graduates:

- To contribute to the economic development of New Jersey and the nation through the ethical practice of engineering;
- To become successful in their chosen career path, whether it is in the practice of engineering, in advanced studies in engineering or science, or in other complementary disciplines;
- To assume leadership roles in industry or public service through engineering ability;
- To maintain career skills through life-long learning and be on the way towards achieving professional licensure.

## **Electrical and Computer Engineering Program Outcomes**

*(What TCNJ Electrical and Computer Engineering students are expected to know and be able to do at graduation. What knowledge, abilities, tools and skills the programs give the graduates to enable them to accomplish the Educational Objectives)*

The Program Outcomes listed below are expected of all graduates of the Electrical or Computer Engineering Program.

**ECE graduates will have:**

- a. **an ability to apply knowledge of mathematics, science and engineering;**  
Students use binary math and Boolean algebra in homework problems, projects, and exams.
- b. **an ability to design and conduct experiments, as well as to analyze and interpret data;**  
Students perform projects that involve experimental hardware setups.
- c. **an ability to design a system, component, or process to meet desired needs;**  
Students perform projects that involve design.
- d. **an ability to function in multidisciplinary teams;**  
Students do projects in teams that can involve EE, CoE, ME, and BME majors.
- e. **an ability to identify, formulate and solve engineering problems;**  
Students perform projects that involve the solution of engineering problems.
- f. an understanding of professional and ethical responsibility;
- g. **an ability to communicate effectively;**  
Students write three Project Reports.
- h. the broad education necessary to understand the impact of engineering solutions in a global and societal context;
- i. a recognition of the need for and an ability to engage in life-long learning;
- j. a knowledge of contemporary issues;
- k. **an ability to use the techniques, skills and modern engineering tools necessary for engineering practice;**  
Students use the Xilinx ISE design tools, ModelSim, FPGAs, and CPLDs.

## Course Objectives:\*

- Objective 1 To understand number system representations, binary codes, binary arithmetic and Boolean algebra, its axioms and theorems, and its relevance to digital logic design. [a, e]
- Objective 2 To understand and apply the representations, design methodologies, and computer-aided design tools for combinational and sequential circuits. [c, e, k]
- Objective 3 To introduce the student to digital systems design using State Machine design, CMOS Logic and a hardware description language like VHDL or Verilog. [c, e, k]
- Objective 4 To expose students to laboratory safety, group interaction, and technical writing. [b, d, g]

## Topics Covered:

1. Design and Analysis
2. Binary Systems and Logic Circuits
3. Boolean Algebra and Mapping Methods
4. Logic Function Realization with MSI Circuits
5. Flip-Flops, Counters, and Registers
6. State Machines
7. Synchronous State Machine Design
8. Interfacing and Design of Synchronous Systems
9. Analog-to-Digital and Digital-to-Analog Converters
10. Digital Hardware
11. First concepts in VHDL or Verilog
12. CMOS Logic Circuits

## Evaluation:

- A. Examinations
- B. Homework
- C. Laboratory/Design Reports
- D. Group Activities

## Performance Criteria:\*\*

### Objective 1

1. Students will demonstrate knowledge of binary number theory, Boolean algebra and binary codes. [A, B, C]
2. Students will understand MSI-level combinational logic components such as adders, decoders, encoders and multiplexers. [A, B, C]
3. Students will understand MSI-level sequential logic components such as registers, shift registers and counters. [A, B, C]

### Objective 2

1. Students will understand and apply the methods of sequential logic design, starting with a high-level problem specification. [A, B, C]
2. Students will understand and be able to explain the basic operation and organization of a computer including fetch-decode-execute, SPU, input/output, memory, bus, etc. [A, B]
3. Students will have an introduction to hardware description language programming. [A, C]

### Objective 3

1. Students will be able to design and analyze synchronous finite state machines and their use in controllers and embedded systems. [A, B, C]
2. Students will understand and be able to apply the representations, design methodologies and computer-aided design tools for combinational and sequential circuits. [A, B, C]

### Objective 4

1. Students must demonstrate that they can work effectively in teams and communicate experimental results clearly. [C, D]

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\* Small letters in brackets refer to the Program Outcomes

\*\* Capital letters in brackets refer to the evaluation methods used to assess student performance

## ENG 312: ADDITIONAL INFORMATION

### 1. DESCRIPTION OF DESIGN ACTIVITY

In the lab/design portion of this course, students start by getting familiar with the tools for digital logic circuits analysis and design. This portion of the course then culminates in a design experience, which comprises of the design of a state machine.

### 2. ENGINEERING STANDARDS

ASCII code and schematic symbols for logic gates.

### 3. REALISTIC CONSTRAINTS

**Economic:** Throughout the course, the economic tradeoffs between the different levels of integration of components used in digital logic design are addressed and discussed.

**Health and Safety:** By working portions of this course in a lab environment and with hardware beyond that represented by a personal computer, students get an appreciation for working with equipment, in groups, and for the health and safety issues associated with working in such environment.

### 4. MODERN AND PROFESSIONAL ENGINEERING TOOLS USAGE

There is a main set of software tools used in this course. It is the Xilinx design package for Field Programmable Gate Arrays (FPGAs), which students use to design and simulate the design assignments of the course.

### 5. COMPUTER USAGE

Students use computers during the lab and design portions of the course to run the engineering tools, and to prepare reports on lab, design, and reading assignments.

### 6. FEEDBACK MECHANISMS

**Homework:** Homework problems are assigned and graded. Not all the problems are graded. These are selected randomly, but students do not know in advanced which problems are going to be graded, so they are behooved to do all assigned problems. These problems are a mixture of analysis and design problems.

**Examinations:** Students are given three partial examinations and a comprehensive final one.

**Laboratory and Design Reports:** Students are graded on laboratory and design reports, which include not only the technical aspects, but also the level of communication skills. There are at least two lab assignments and one design assignment.