

ENG 312 - PROJECT #3

SEQUENTIAL LOGIC DESIGN

In this project, the students will obtain experience with sequential logic design, and study digital design using the Xilinx design package for FPGAs and CPLDs. The digital design will be evaluated using a Xilinx FPGA. This project builds on Projects #1 and #2. It is assumed that the students have performed the Xilinx tools tutorials from Project #1, and all the reading in parts 1-3 in Project #2. If this material is not clear, the students should go back and repeat these steps in Projects #1 and #2. There is an example controller in this project handout.

1. Design a controller that detects the four-bit, binary MSB first serial sequence of the rounded average of the last digits of the team members' Social Security Numbers. You should use the clock signal provided in the Spartan-3E Starter Kit board. The input bit should be setup before the clock pulse.
2. Implement the design with the Spartan-3E Xilinx FPGA with the Starter Kit board clock set at the slowest clock rate possible.
3. Write a report, which will be due on the last meeting session of the course, that contains at a minimum the following:
 - a. The corresponding state diagram. What is the digit that you are trying to detect?
 - b. Your Verilog® design code. Use:
 - i. Device Family: Spartan 3E
 - ii. Device: XC3S500E
 - iii. Package: FG320
 - iv. Speed: -5
 - c. Your Verilog® Test Bench design code. If necessary, add ```timescale 1ns/1ps` as the first line of your test bench file, and comment out the ```ifdef` and ```endif`

lines.

- d. The waveforms resulting from the verification of your design.
 - e. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints. Use a clock period of 1 μ S as the timing constraint.
 - f. Snapshot of the routed design.
 - g. Post Place and Route timing report.
 - h. First page of the IBIS model of your design.
 - i. What is the maximum frequency at which your design can run?
 - j. Proof that instructor has reviewed the Xilinx implementation.
4. GRADING RUBRIC: The total grade for this assignment will be 11 points normalized to 100% for your report. Point (a) in (3) will be worth 2 points, points (b) through (i) in (3) will be worth 1 point each, and 1 point for a sheet of blank paper that will be in your report where the instructor has signed verifying that he has seen your design working in the FPGA board.
5. REPORT FORMAT: Free form, but it must be:
- a. One report per team.
 - b. Have a cover sheet with identification: Title, Class, Your Name, etc.
 - c. COMPLETELY word-processed
 - d. Double spaced
 - e. 12 pt Times New Roman font
 - f. Fully justified (optional)

```

module controller1(x,clk,rstn,y,z);
    input x;
    input clk;
    input rstn;
    output y;
    output z;

    parameter S0 = 3'h0, S1 = 3'h1, S2 = 3'h2, S3 = 3'h3, S4 = 3'h4;

    reg [2:0] PRState, NXState;
    reg y;

    assign z = ~y;

    always @ (PRState) begin
        if (PRState == S4) y = 1'b1;
        else y = 1'b0;
    end

    always @ (posedge clk or negedge rstn) begin
        if (rstn == 1'b0) PRState = S0;
        else PRState = NXState;
    end

    always @ (PRState or x) begin
        case (PRState)
            S0 : if (x == 1'b0) NXState = S1;
                 else NXState = S0;
            S1 : if (x == 1'b0) NXState = S2;
                 else NXState = S1;
            S2 : if (x == 1'b1) NXState = S3;
                 else NXState = S2;
            S3 : if (x == 1'b0) NXState = S4;
                 else NXState = S3;
            S4 : NXState = S4;
        endcase
    end

endmodule

```