# ENG 312 - PROJECT #2

# COMBINATIONAL LOGIC DESIGN

In this project, the students will study digital design using the Xilinx design package for FPGAs and CPLDs, and SSI Logic Gates. The digital design will be evaluated using a Xilinx FPGA, and it will be verified using SSI logic gates. Additionally, the students will become familiar with the electronic digital design components and their specifications.

1. Obtain and go through the "Principles of Functional Verification" write-up available at http://www.tcnj.edu/~hernande/ELEC451/0750676175.pdf. Do not print this write-up in this lab. Use Acrobat to view it instead.
2. Obtain and go through the "Spartan-3E FPGA Family Data Sheet" available at http://www.tcnj.edu/~hernande/Eng312/ds312.pdf. Do not print this data sheet in this lab. Use Acrobat to view it instead.
3. Obtain and go through the "Spartan-3E Starter Kit Board User Guide" available at http://www.tcnj.edu/~hernande/Eng312/S3EStarter_ug230.pdf. Do not print this manual in this lab. Use Acrobat to view it instead.
4. Design a combinational circuit that counts the coins placed into an automatic toll coin collector. The toll is $0.10 and the machine gives no change. When at least $0.10 are received the go-signal is turned on and the money collected (no change is given). Otherwise the stop-light remains on.
5. Implement the design with the XC3S500E Xlinx FPGA.
6. Implement the design with a breadboard using SSI parts.
7. Write a report, which will be due by the date announced in class, that contains the following:
    a. Toll collector scheme including any mechanical components.
    b. Your Verilog® design code. Use:

i. Device Family: Spartan 3E

ii. Device: XC3S500E

iii. Package: FG320

iv. Speed: -5

c. Your Verilog® Test Bench design code. Use "`` `timescale 1ns/1ps ``" as the first line of your test bench file, and comment out the "`` `ifdef ``" and "`` `endif ``" lines.

d. The waveforms resulting from the verification of your design with ModelSim.

e. The design schematic from the Xilinx synthesis of your design. Do not use any timing or area constraints.

f. Snapshot of the routed design.

g. Post Place and Route timing report.

h. First page of the IBIS model of your design.

i. Proof that instructor has reviewed the Xilinx and SSI implementations.

8. GRADING RUBRIC: The total grade for this assignment will be 10 points normalized to 100% for your report. Points (a) through (h) in (9) will be worth 1 point each, and 1 point each for sheets of blank paper that will be in your report where the instructor has signed verifying that he has seen your design working in the FPGA board and with SSI parts.

9. REPORT FORMAT: Free form, but it must be:

a. One report per team. A team is two people.

b. Have a cover sheet with identification: Title, Class, Your Name, etc.

c. COMPLETELY word-processed

d. Double spaced

e. 12 pt Times New Roman font

f. Fully justified (optional)