ENG 312 - PROJECT #1

INTRODUCTION TO XILINX

In this project, the students will become familiar with the operation of the Xilinx design package for Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs).

1. Go through the on-line presentation "ISE 8.2i Software Interactive Tutorial for Xilinx PLDs" available at http://www.tcnj.edu/~hernande/movies/xilinx1.html.
2. Obtain and go through Chapters 1, 2, 4, and 5 of the "Xilinx ISE 7 In-Depth Tutorial" available at http://www.tcnj.edu/~hernande/Eng312/ise7tut.pdf, along with the Verilog® design files available at http://www.tcnj.edu/~hernande/Eng312/wtut_ver.zip. Copy the files to your own disk space. Do not put files locally in the machines. Do not print this tutorial in this lab; it is about 160 pages long. Use Acrobat to view it instead.
3. Write a report, which will be due by the date announced in class, commenting and discussing:
    a. The purpose and use of the software package in digital design.
    b. The ease of use of Xilinx' ISE tool for digital design and evaluation.
    c. The information that can be obtained about a digital design using Xilinx' ISE.
    d. What part of the digital design process can be accomplished with Xilinx' ISE and which part(s) cannot?
    e. Possibility of using Xilinx and a suitable FPGA or CPLD board to process electrical analog data. Describe your scheme.
4. GRADING RUBRIC: The total grade will be 7 points normalized to 100% for your report. Points a through c in (3) will be worth 1 point each, and points d and e will be worth 2 points each.
5. REPORT FORMAT: Free form, but it must be:
    a. One report per team

b. Have a cover sheet with identification: Title, Class, Your Names, etc.

c. COMPLETELY word-processed

d. Double spaced

e. 12 pt Times New Roman font

f. Fully justified (optional)