ELC 363 - LABORATORY #5

MIPS ALU

In this laboratory, the MIPS ALU will be implemented and verified in Verilog® using an as high as possible level of abstraction design methodology. This implementation will only have to support the following instructions (simplified ISA):

- arithmetic-logical instructions:
  - add, sub, and, or, slt
- control flow instructions:
  - beq

The design approach should be bottoms-up starting with the top portion of Fig. 1 as a guide and Fig. 2. This implementation will not support overflow detection.

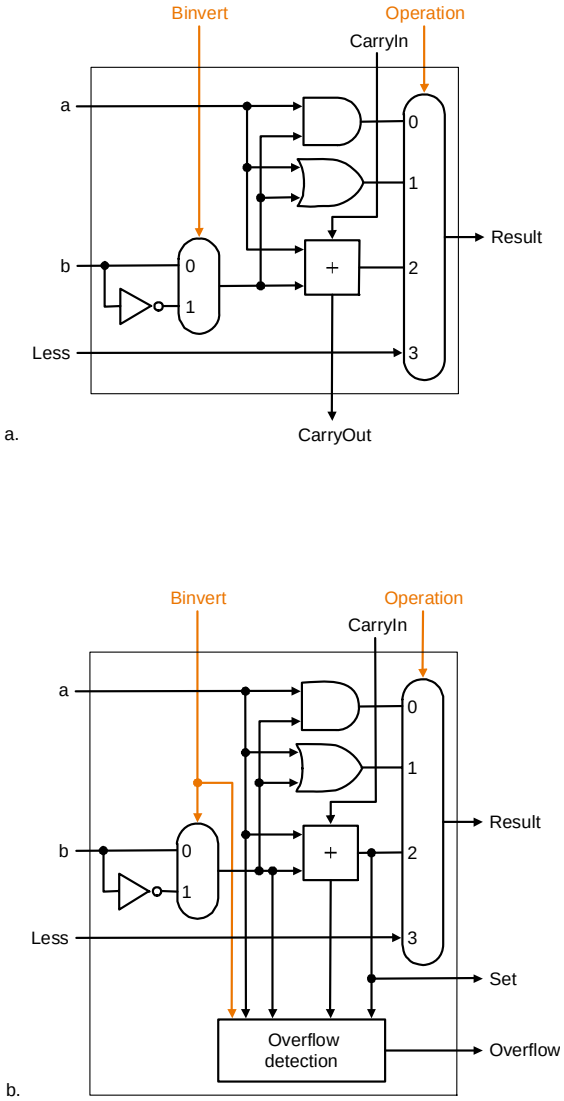

Fig. 1. ALU 1-Bit Slice

- Notice control lines:

```
000 = and
001 = or
010 = add
110 = subtract
111 = slt
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•***Note: zero is a 1 when the result is zero!***

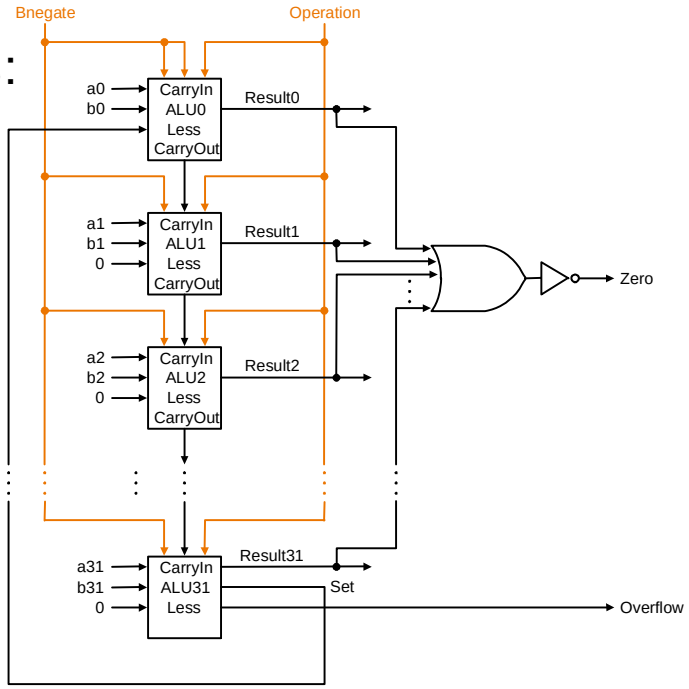

Fig. 2. ALU Architecture

The next step is to write a test bench to verify the design. The minimum deliverables for this laboratory are the following:

a) All Verilog® code.

b) Waveforms that show that the ALU works for all instructions.

A report with, at a minimum, all the items requested to be turned in is to be submitted by each team by the due date discussed in class. All reports should be written in a word processor and similar productivity computer tools; no hand written reports will be accepted.

GRADING RUBRIC: The total grade for this assignment will be 18 points normalized to 100% for your report. Parts (a) and (b) above will be worth 6 points each. The rest of your report will be worth 6 points, for a total of 18 points.

REPORT FORMAT: Free form, but it must be:

a. One report per team.

b. Have a cover sheet with identification: Title, Class, Your Name, etc.

c. COMPLETELY word-processed

d. Double spaced

e. 12 pt Times New Roman font

f. Fully justified (optional)

g. Outline of the body of the report: Introduction, Problem Description, Results, Discussion, and Conclusions.