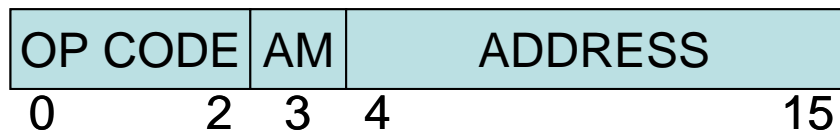


# ELC 363 - LABORATORY #4

## SIMPLE PROCESSOR

In this laboratory, the students will obtain experience with the architecture of a simple processor, and will design the processor using the Xilinx design package for FPGAs and CPLDs.

Consider a simple accumulator based processor with a 16-bit word length, and an instruction word format as shown below.



If AM = 0, the addressing mode is direct, and if AM = 1, the addressing mode is indirect.

The machine has the following registers only.

REGISTER NAME	FUNCTION	LENGTH
IR	INSTRUCTION REGISTER	16 bits
MD	MEMORY DATA REGISTER	16 bits
AC	ACCUMULATOR	16 bits
PC	PROGRAM COUNTER	12 bits
MA	MEMORY ADDRESS REGISTER	12 bits

The processor implements the following instructions only.

OP CODE	MNEMONIC	DESCRIPTION
000	NOT	INVERT
001	ADC	ADD WITH CARRY

OP CODE	MNEMONIC	DESCRIPTION
010	JPA	JUMP IF ACC > 0
011	INCA	INCREMENT ACC
100	STA	STORE AND CLEAR ACC
101	LDA	LOAD ACCUMULATOR

1. Study the supplied architecture that uses a minimum CPI Von Newman approach.
2. Study the supplied controller flow diagram.
3. Design and test the processor in simulations.
4. Implement the design with any Xilinx FPGA with the clock set at 1 MHz.
5. Write a report, which will be due on the day announced in class, that contains at a minimum the following:
  - a. RTL for each instruction and addressing mode combination.
  - b. Number of clock cycles for each instruction and addressing mode combination.
  - c. Your Verilog® design code.
  - d. Your Verilog® Test Bench design code. Use “`timescale 1ns/1ps” as the first line of your test bench file, and comment out the “`ifdef“ and “`endif” lines if they are generated.
  - e. Your assembly language test program. All instructions and addressing mode combinations need to execute at least once.
  - f. Your machine language test program.
  - g. The waveforms resulting from the verification of your design.
  - h. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints. Use a clock period of 1 μS as the timing constraint.

- i. Snapshot of the routed design.
- j. Post Place and Route timing report.
- k. First page of the IBIS model.

#### 6. GRADING RUBRIC:

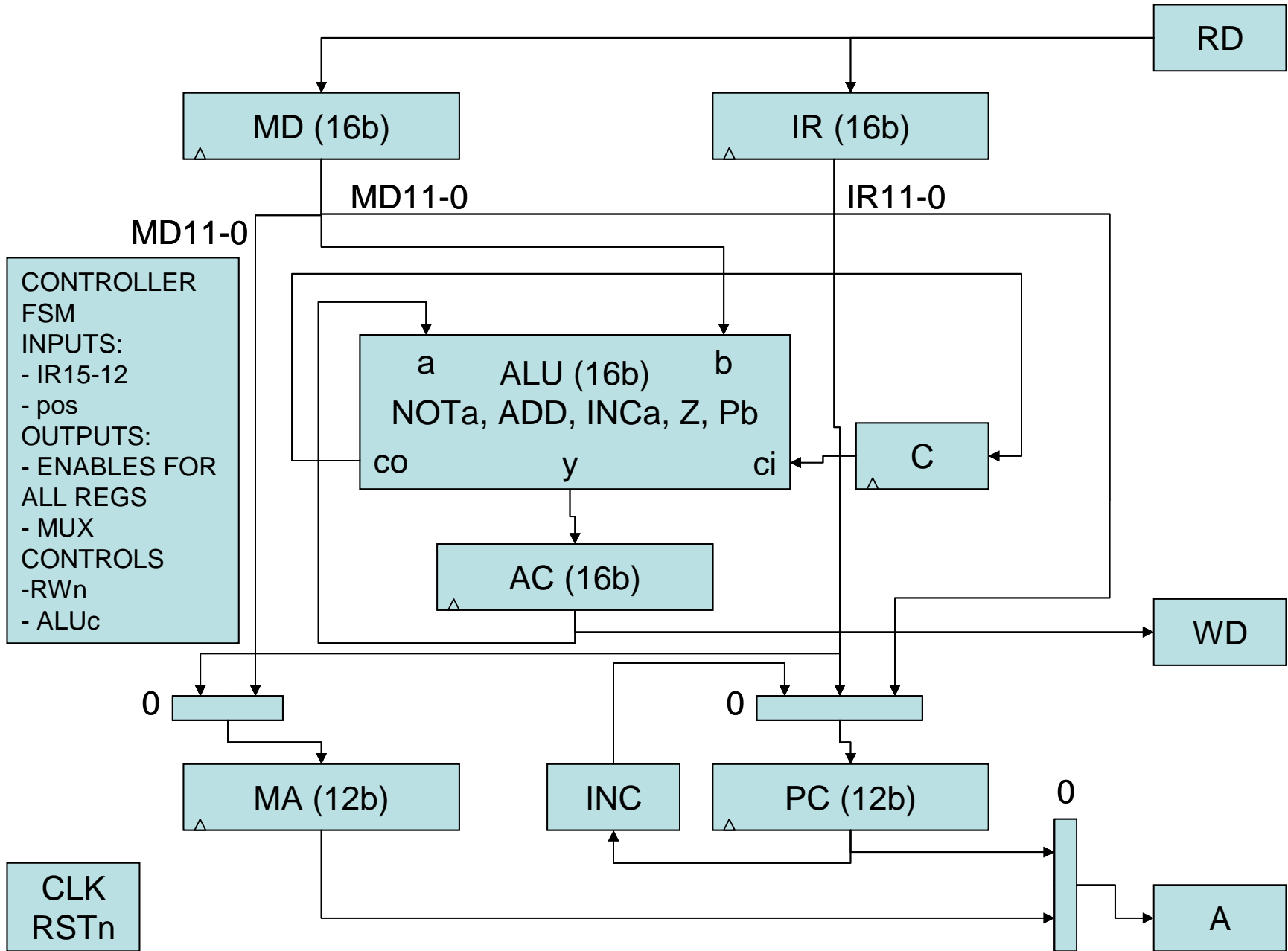
The total grade for this assignment will be 58 points normalized to 100% for your report. Items 5.a-c will be worth 12 points each, 5.d-g will be worth 4 points each, and 5.h-k will be worth 1 point each. The rest of the report will be worth 6 points, for a total of 58 points.

#### 7. REPORT FORMAT:

Free form, but it must be:

- a. One report per team.
- b. Have a cover sheet with identification: Title, Class, Names, etc.
- c. COMPLETELY word-processed
- d. Double spaced
- e. 12 pt Times New Roman font
- f. Fully justified (optional)
- g. Outline of the body of the report: Introduction, Problem Description, Results, Discussion, and Conclusions.

Architecture:



Controller flow diagram:

