ELC 363 - LABORATORY #2

SEQUENTIAL LOGIC DESIGN

In this project, the students will obtain experience with sequential logic design, and study digital design using the Xilinx design package for FPGAs and CPLDs. This project builds on Projects #1. It is assumed that the students have performed the Xilinx tools tutorials from Project #1. If this material is not clear, the students should go back and repeat these steps in Projects #1. There is an example controller in this project handout.

1. Design a controller that detects the four-bit, binary MSB first serial sequence of the rounded average of the last digits of the team members' Social Security Numbers. The input bit should be setup before the clock pulse.
2. Implement the design with the XC2S50 Xlinx FPGA.
3. Write a report, which will be due on the last meeting session of the course, that contains at a minimum the following:
    a. The corresponding state diagram. What is the digit that you are trying to detect?
    b. Your Verilog® design code. Use:
        i. Device Family: Spartan2
        ii. Device: XC2S50
        iii. Package: TQ144
        iv. Speed: -5
    c. Your Verilog® Test Bench design code. If necessary, add "`` `timescale 1ns/1ps ``" as the first line of your test bench file, and comment out the "`` `ifdef ``" and "`` `endif ``" lines.
    d. The waveforms resulting from the verification of your design with ModelSim.

e. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints. Use a clock period of 1 μS as the timing constraint.

f. Snapshot of the routed design.

g. Post Place and Route timing report.

h. First page of the IBIS model of your design.

i. What is the maximum frequency at which your design can run?

4. GRADING RUBRIC: The total grade for this assignment will be 10 points normalized to 100% for your report. Point (a) in (3) will be worth 2 points and points (b) through (i) in (3) will be worth 1 point each.

5. REPORT FORMAT: Free form, but it must be:

    a. One report per team.

    b. Have a cover sheet with identification: Title, Class, Your Name, etc.

    c. COMPLETELY word-processed

    d. Double spaced

    e. 12 pt Times New Roman font

    f. Fully justified (optional)

```
module controller1(x,clk,rstn,y,z);
    input x;
    input clk;
    input rstn;
    output y;
    output z;

  parameter S0 = 3'h0, S1 = 3'h1, S2 = 3'h2, S3 = 3'h3, S4 = 3'h4;

  reg [2:0] PRState, NXState;
  reg y;

  assign z = ~y;

  always @ (PRState) begin
    if (PRState == S4) y = 1'b1;
    else y = 1'b0;
  end

  always @ (posedge clk or negedge rstn) begin
    if (rstn == 1'b0) PRState = S0;
    else PRState = NXState;
  end

  always @ (PRState or x) begin
    case (PRState)
      S0 : if (x == 1'b0) NXState = S1;
               else NXState = S0;
      S1 : if (x == 1'b0) NXState = S2;
               else NXState = S1;
      S2 : if (x == 1'b1) NXState = S3;
               else NXState = S2;
      S3 : if (x == 1'b0) NXState = S4;
               else NXState = S3;
      S4 : NXState = S4;
    endcase
  end

endmodule
```