

Figure 9.45 Phase detector

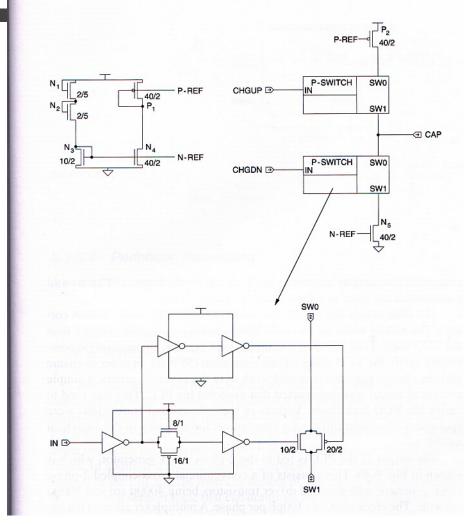


FIGURE 9.46 Charge pump



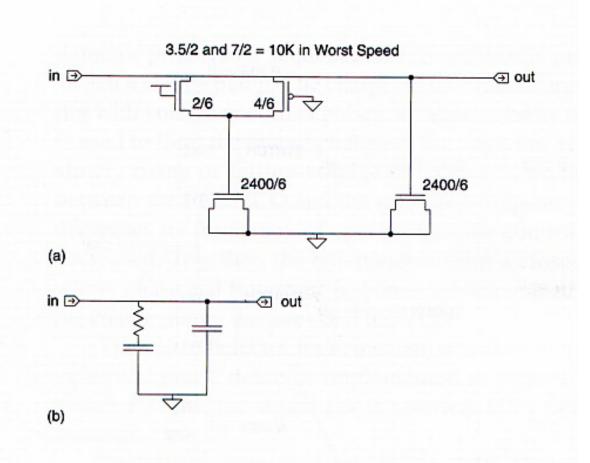
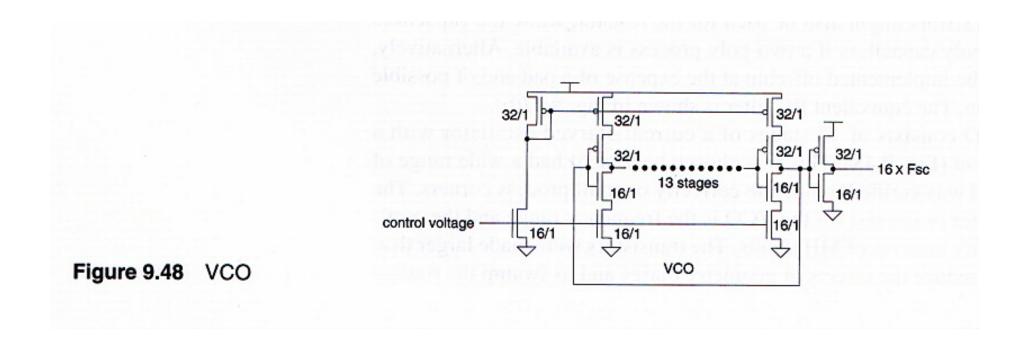
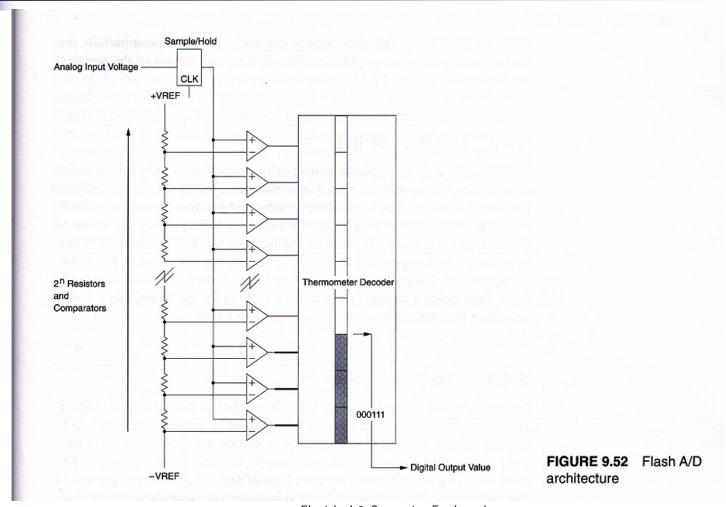


Figure 9.47 Filter



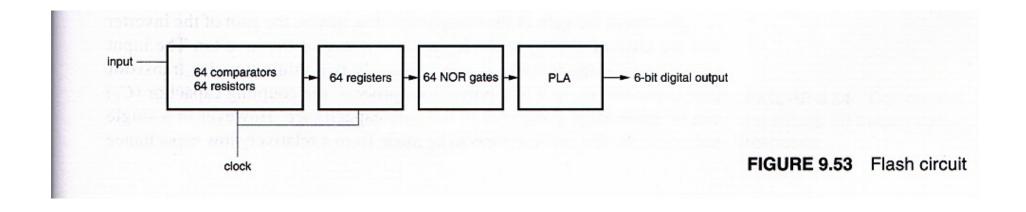


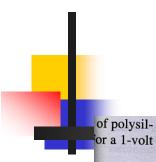


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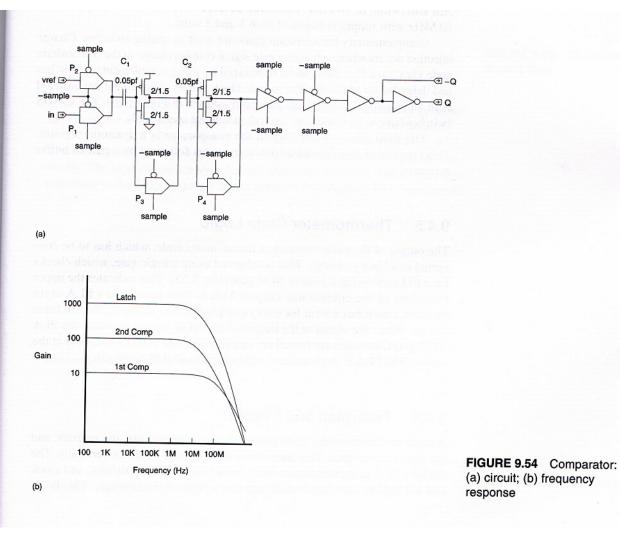


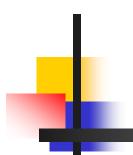


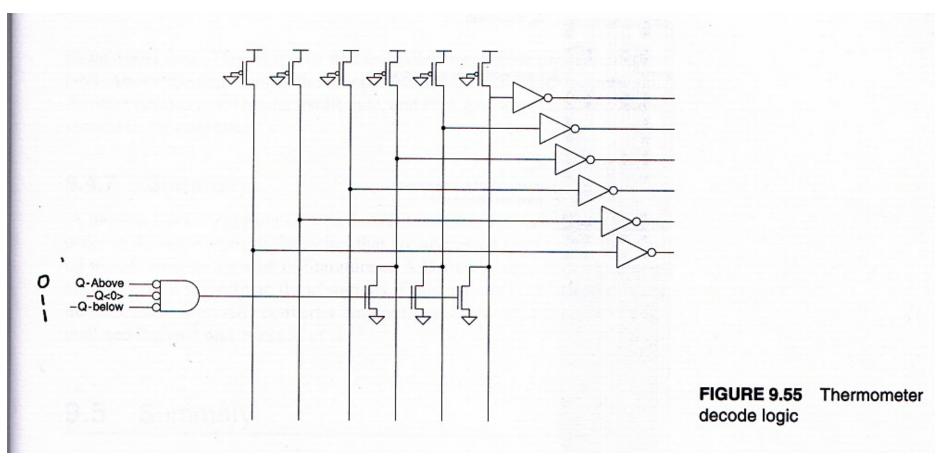
ed, capaciister. Dur-'1 via pass id P<sub>4</sub>. The present in erent charto slightly eroed, the -zero step

capacitor, a voltage put of the in of the pacitance mparator.

e inverter Fhe input transistor citor  $(C_1)$  a single pacitance







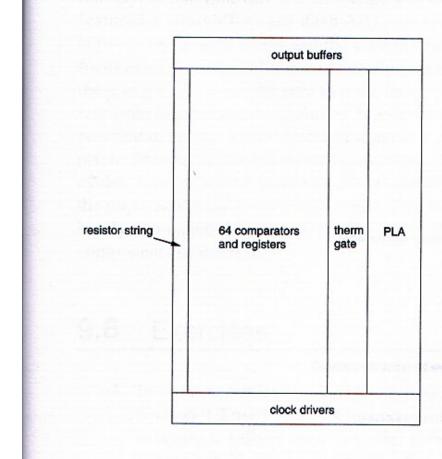
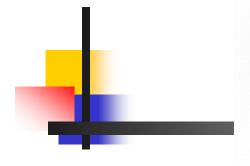


FIGURE 9.56 Floorplan of A/D



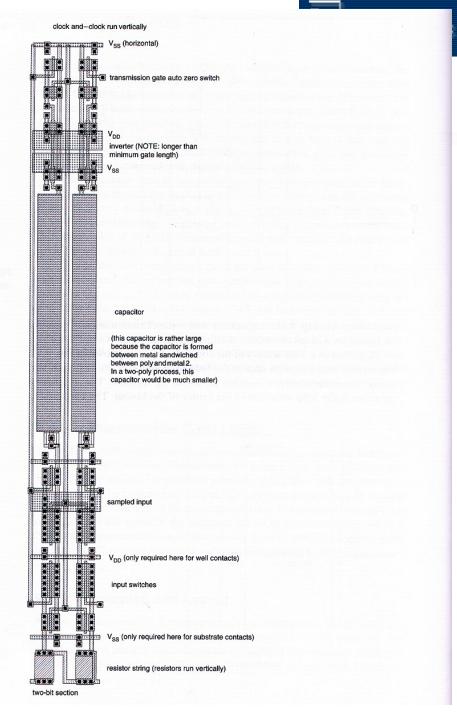
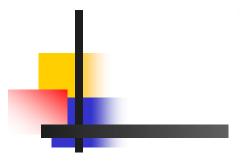
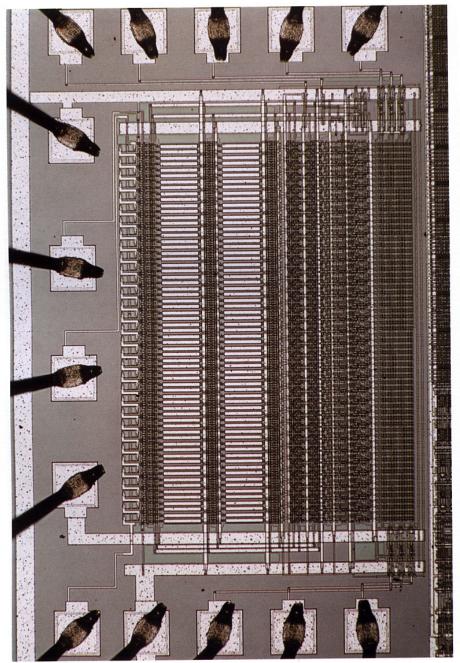


FIGURE 9.57 Partial cell layout for A/D







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