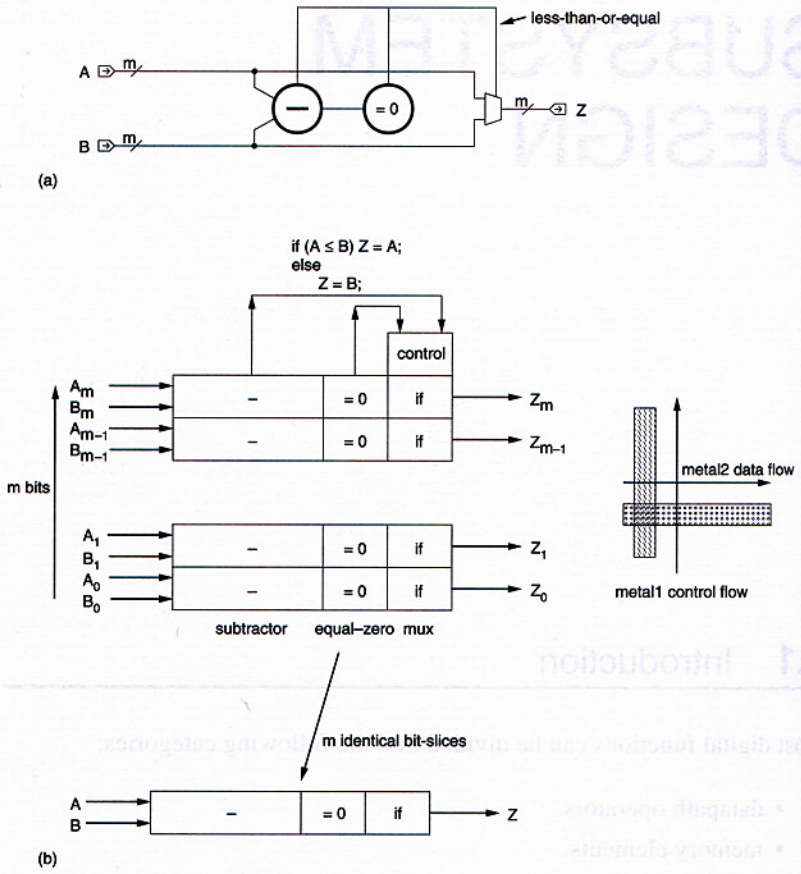


FIGURE 8.1 Datapath Example

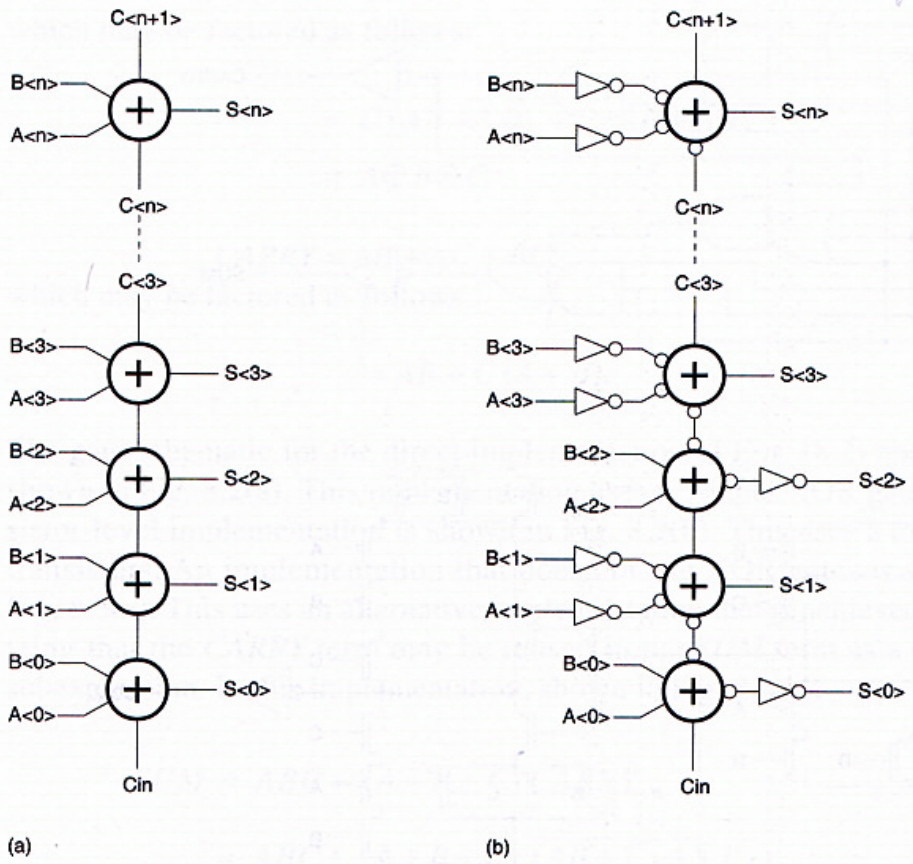


Figure 8.4 Parallel adder implementations

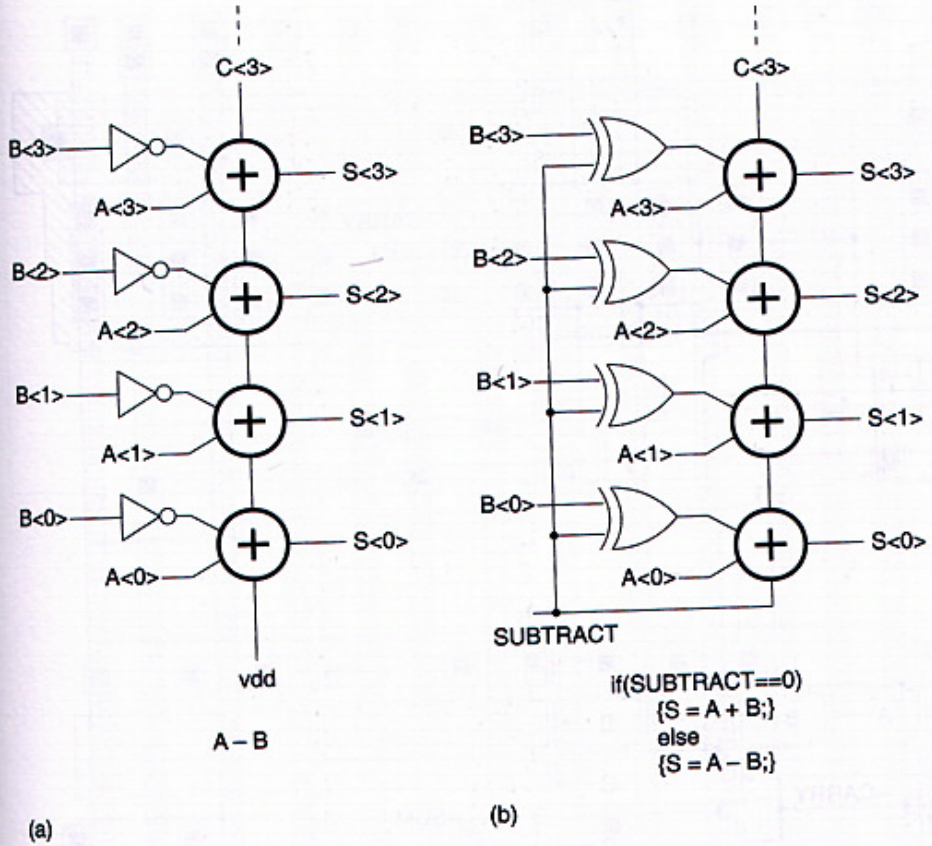
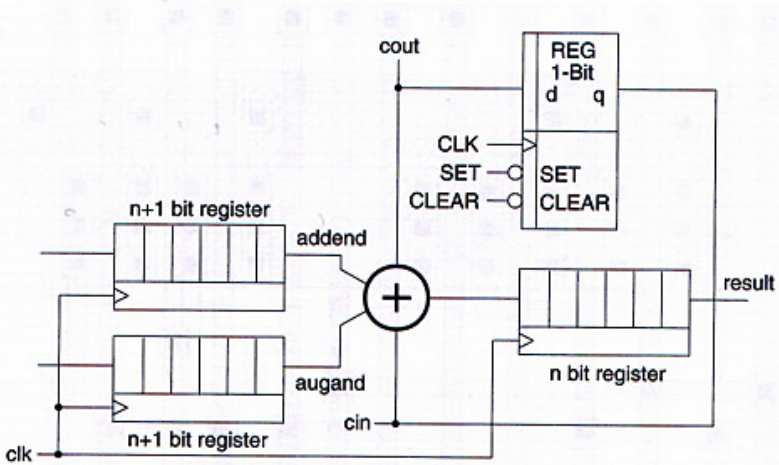


FIGURE 8.5 Arithmetic operators: (a) subtractor; (b) adder/subtractor



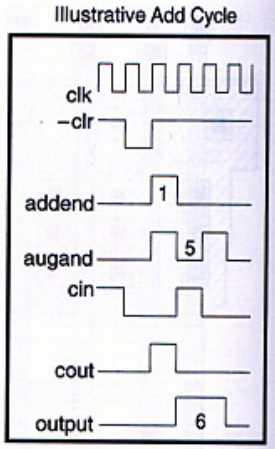


Figure 8.8 Bit-serial adder implementation

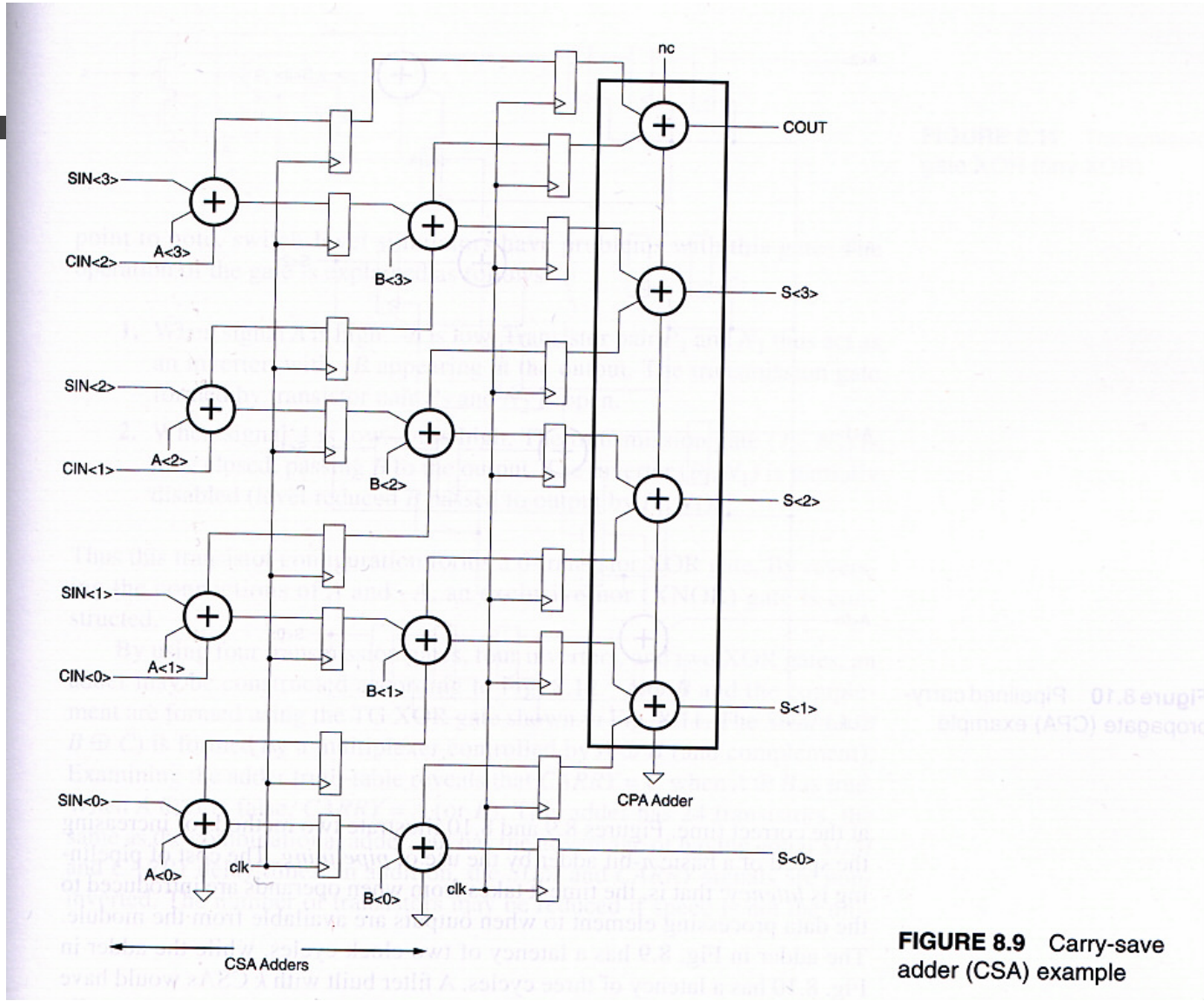


FIGURE 8.9 Carry-save adder (CSA) example

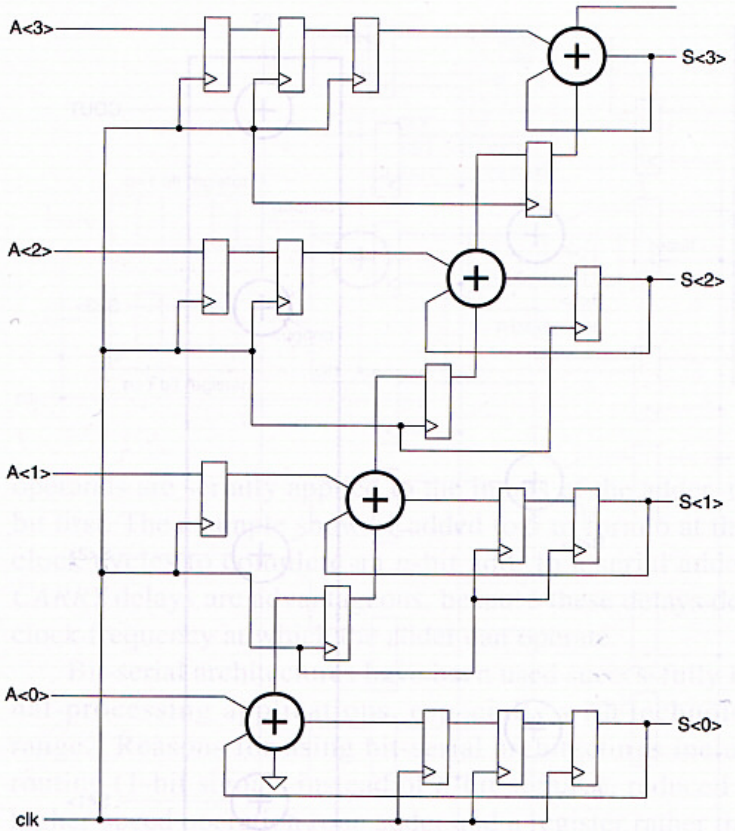


Figure 8.10 Pipelined carry-propagate (CPA) example

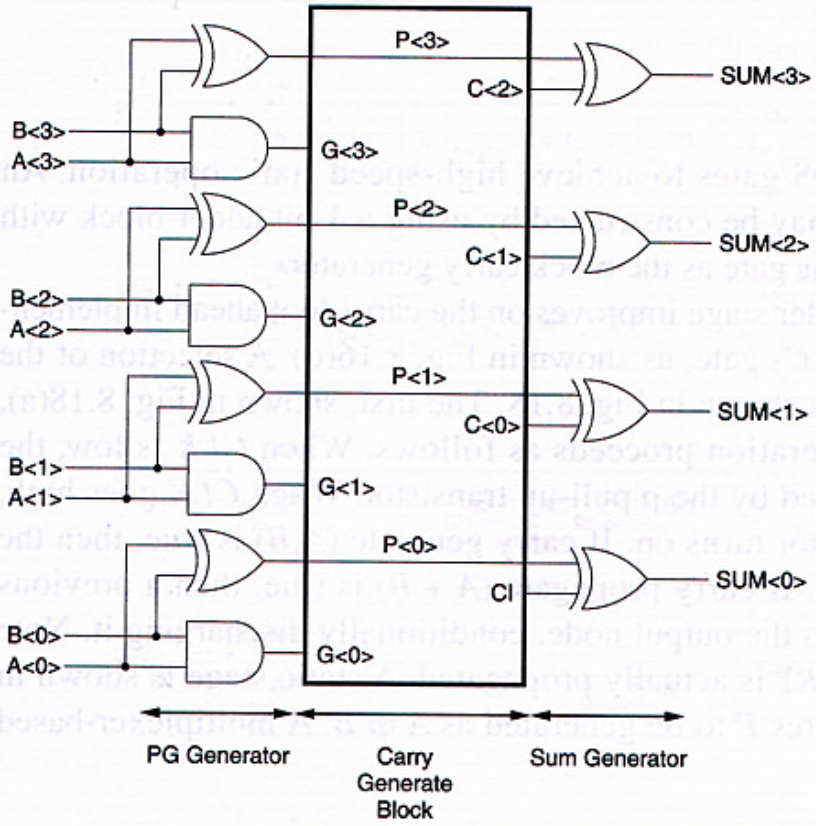


FIGURE 8.14 Generic carry-lookahead adder (CLA)

TABLE 8.2 4-bit Multiplier Partial Products

				X3	X2	X1	X0	Multiplicand
				Y3	Y2	Y1	Y0	Multiplier
				X3Y0	X2Y0	X1Y0	X0Y0	
			X3Y1	X2Y1	X1Y1	X0Y1		
		X3Y2	X2Y2	X1Y2	X0Y2			
	X3Y3	X2Y3	X1Y3	X0Y3				
P7	P6	P5	P4	P3	P2	P1	P0	Product

are mn sum-
tes. For 4-bit
2.
dders, and n^2
multiplier is
shows a cell
is propagated

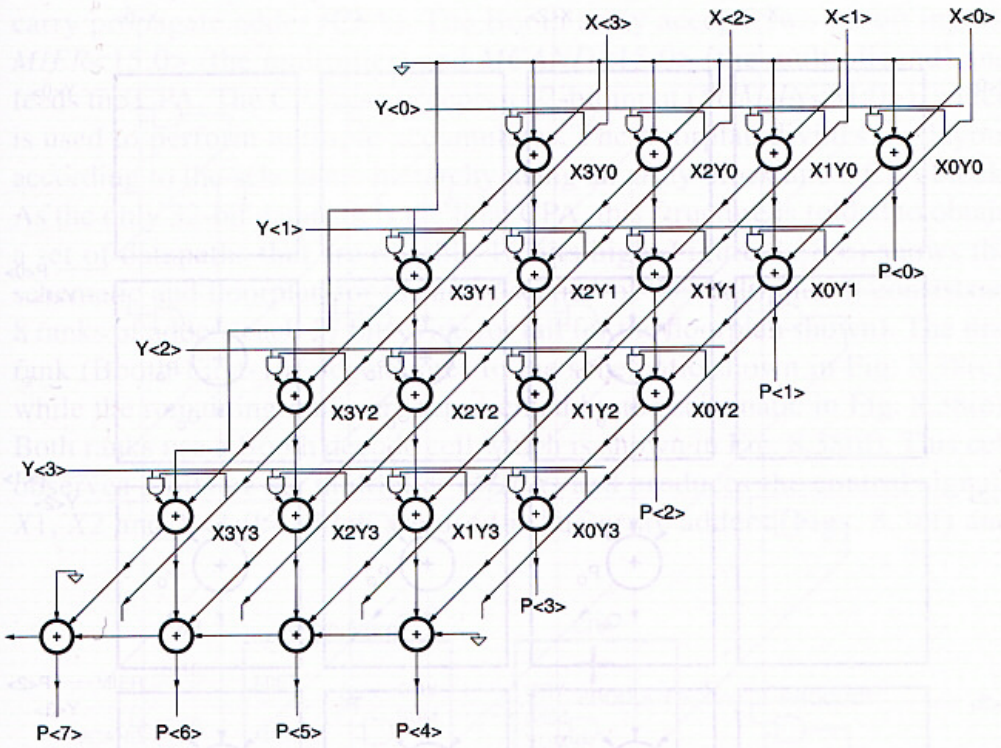


FIGURE 8.36 A 4 × 4 array multiplier

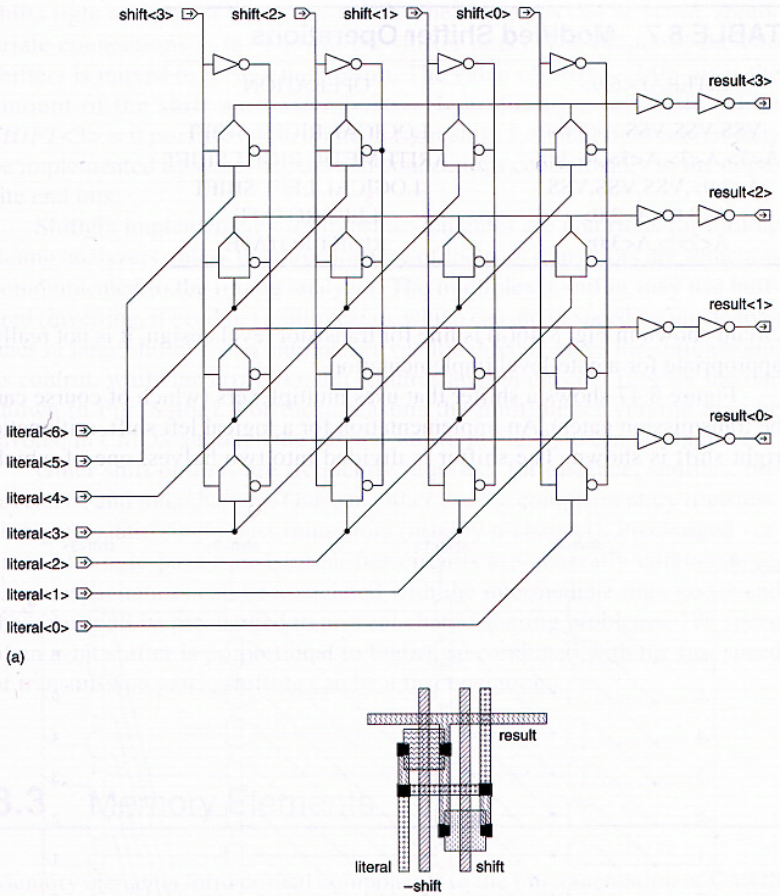


FIGURE 8.46 Array shifter using transmission gates: (a) circuit; (b) cell layout

TABLE 8.6 Shifter Operations

SHIFT	RESULT
1	LITERAL<3:0>
2	LITERAL<4:1>
4	LITERAL<5:2>
8	LITERAL<6:3>

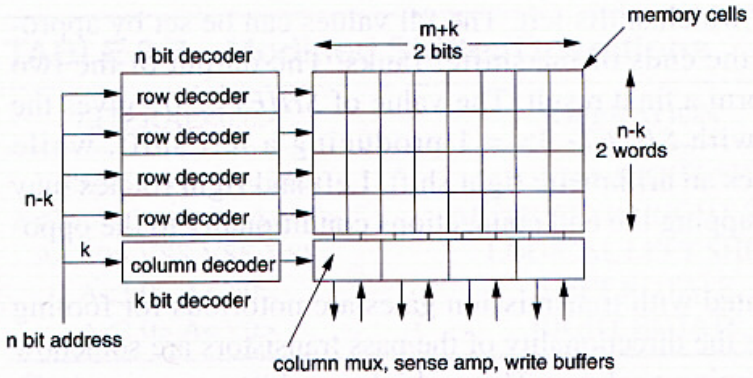


FIGURE 8.48 Memory-chip architecture

ntent-address-
ccess memory,
nemory (com-
h greater than
order of milli-
. Both types of
and asynchro-

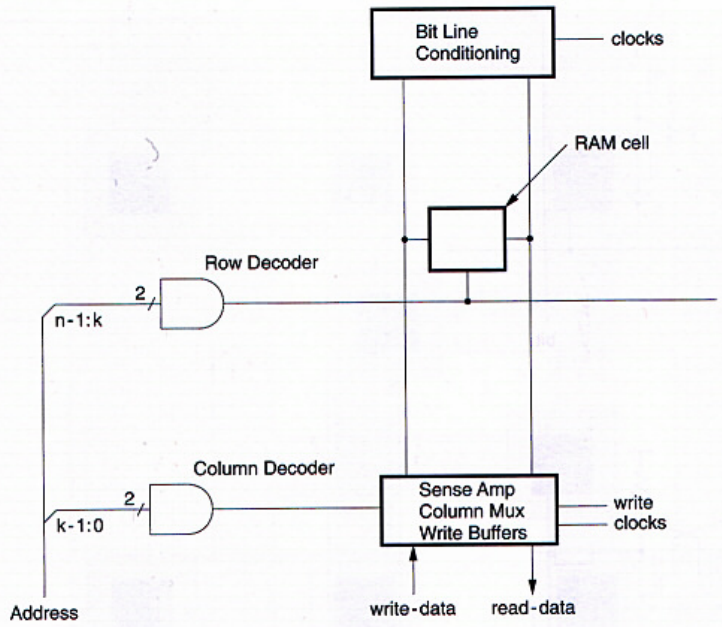


FIGURE 8.49 Generic RAM circuit

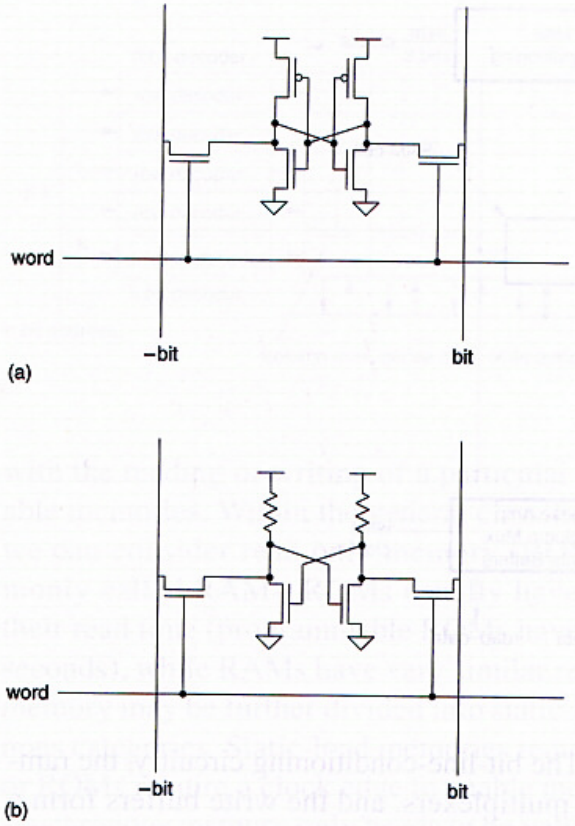


Figure 8.50 Static RAM cell circuits

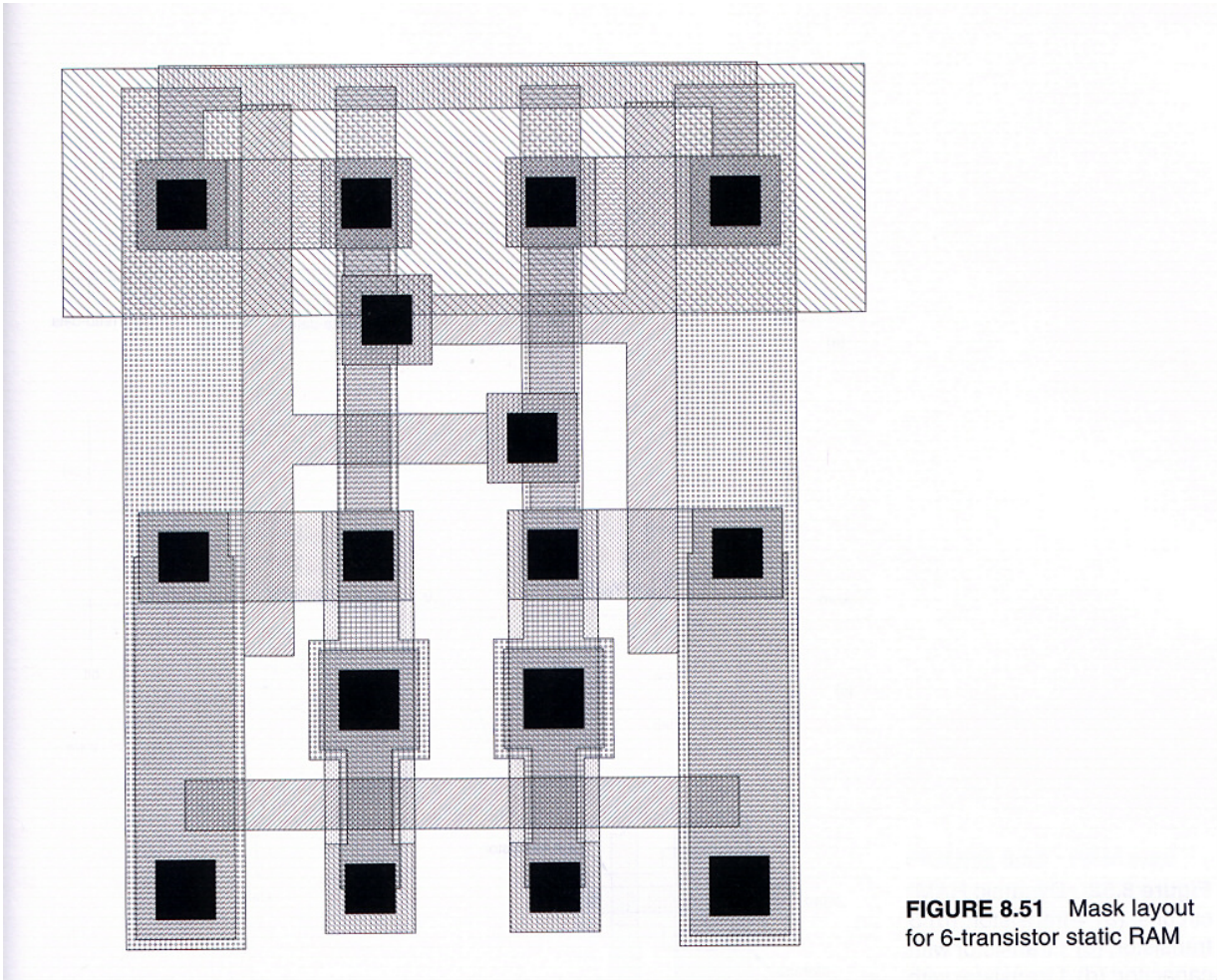
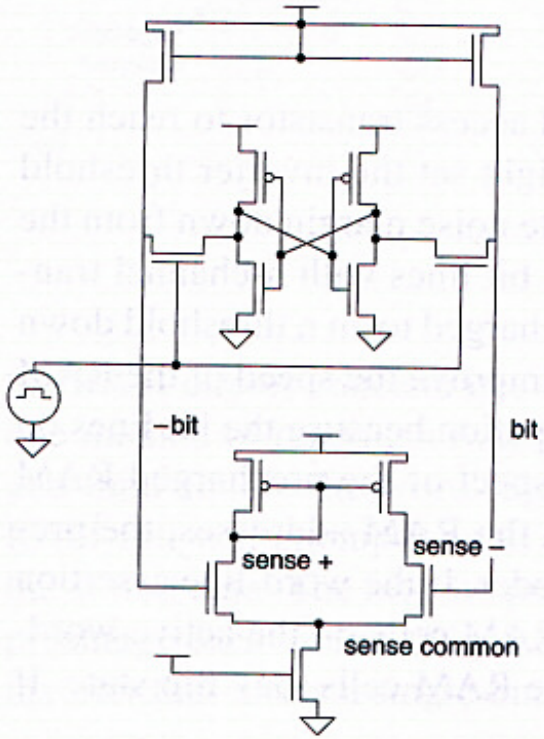
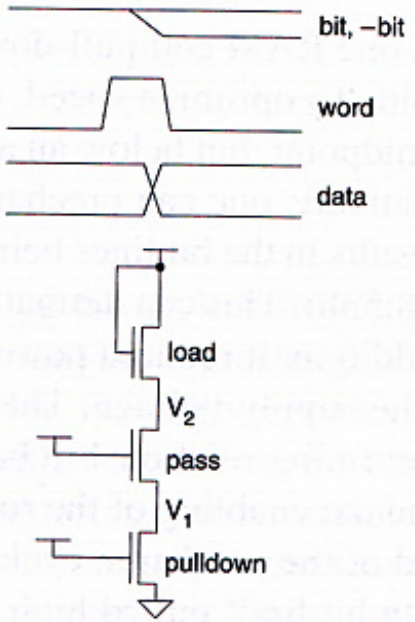


FIGURE 8.51 Mask layout for 6-transistor static RAM



(a)



(b)

Figure 8.54 RAM read operation model

technique, the
. The theory is
in driving the

es to the RAM
during the read
uit. In this cir-
w the data and
serted (actually
s driven to V_{SS},
n V_{DD}. Figure
re shows a zero
e written, node
and at the same
hreshold. In the
he write-access
P_{bit} (the RAM
N_5 (the bit-line
ne side, P_D, N_2
write operations
istors, as shown
ver all process,
ot of the wave-
model the RAM
nd *–write-data*

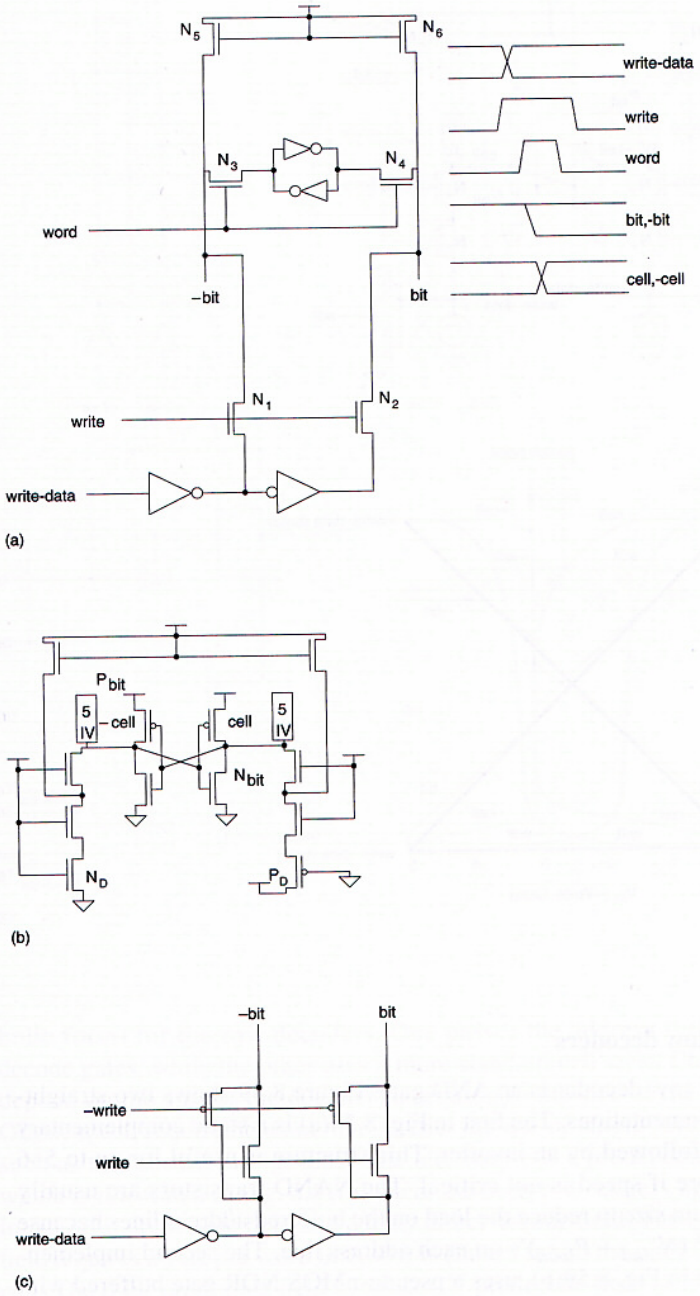


FIGURE 8.57 Static RAM–write circuits: (a) n-channel pass transistors; (b) circuit model during write; (c) complementary transmission gate version

the decoder has
rite operation is
being actively
s. However, the
nt values before
AM, this speed
y sizing transis-
decode signal.

nd write ports.
ng pass transis-

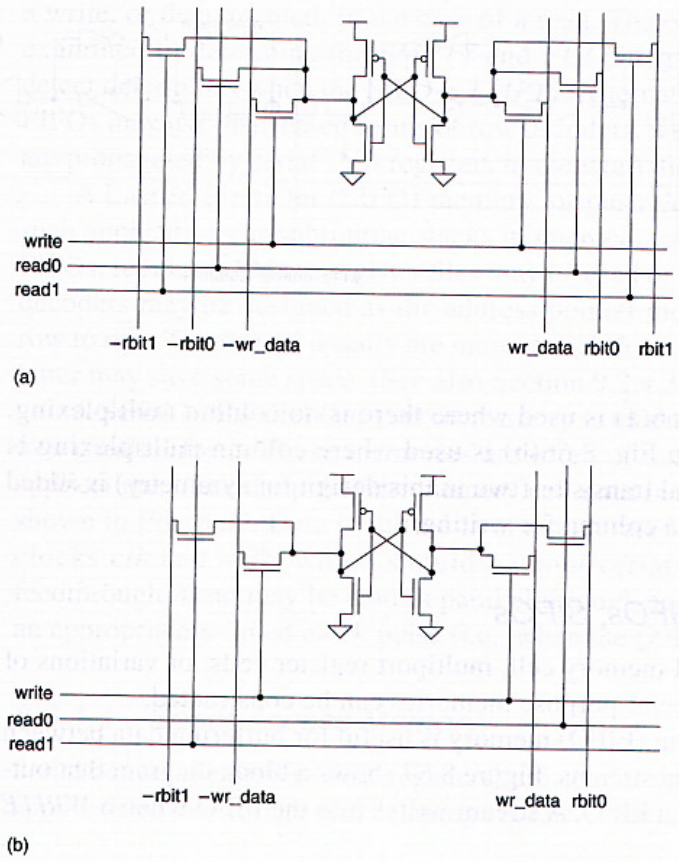


FIGURE 8.65 Multiported (2R-1W) RAM cell: (a) fully differential; (b) single-ended read

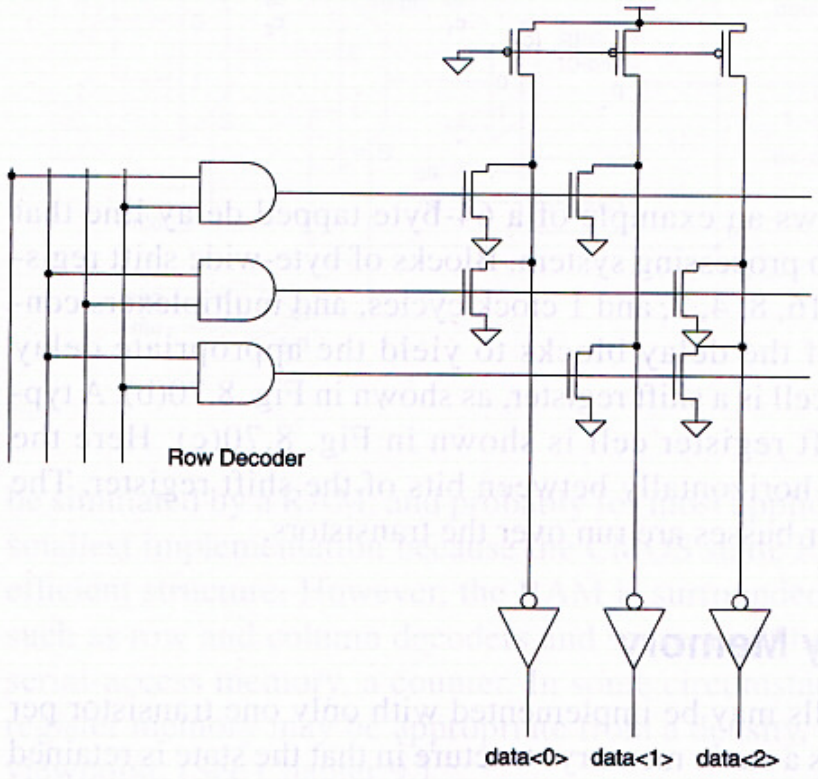


Figure 8.71 Basic ROM architecture

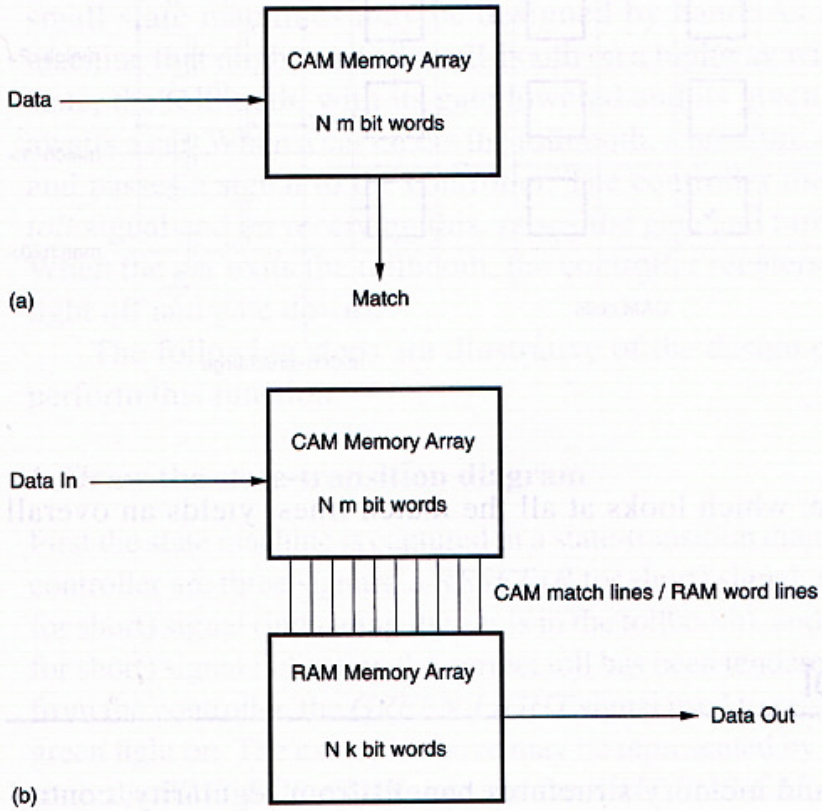


FIGURE 8.75 CAM architecture: (a) basic CAM; (b) typical application as translation lookaside buffer