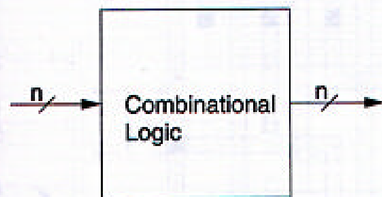
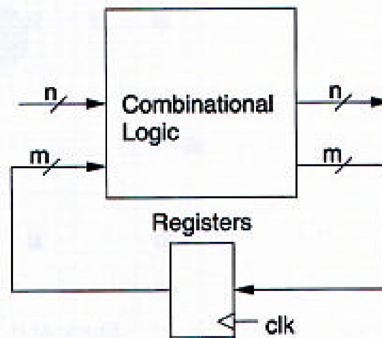


2^n inputs required to exhaustively test circuit

(a)

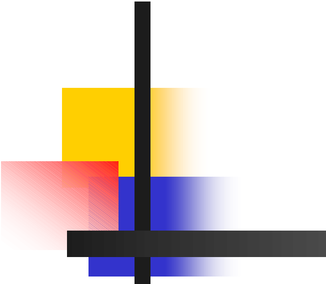


2^{n+m} inputs required to exhaustively test circuit

For n = 25 m = 50, 1μS/test, the test time is over 1 billion years (Williams)

(b)

FIGURE 7.1 The combinational explosion in test vectors



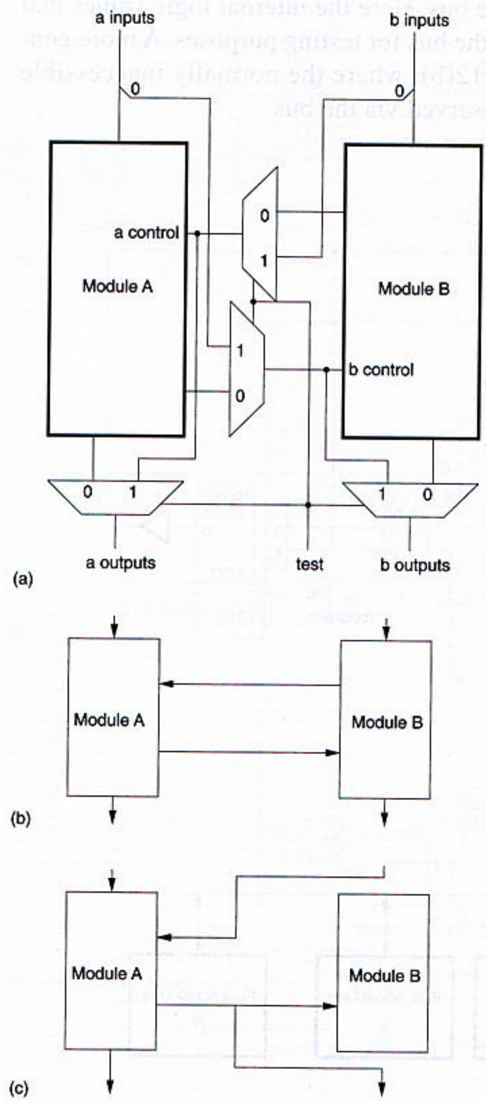


FIGURE 7.13 Multiplexer based testing

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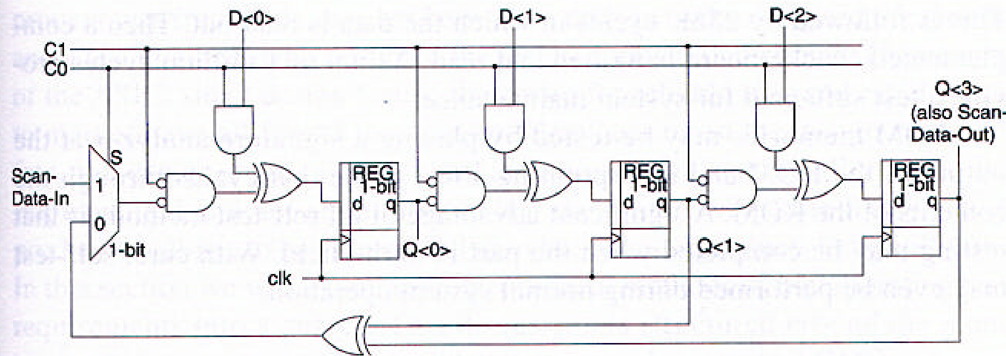
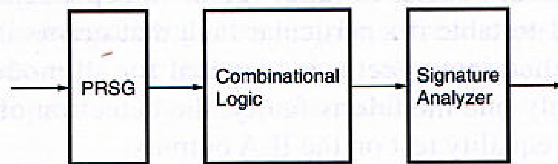


(a)

MODE	C_0	C_1	
A	0	0	Scan Mode
B	0	1	Reset
C	1	0	PRSG or Signature Analyzer
D	1	1	Parallel Registers



(b)

FIGURE 7.22 Built-in logic block observation (BILBO): (a) individual register; (b) use in a system

The College of New Jersey

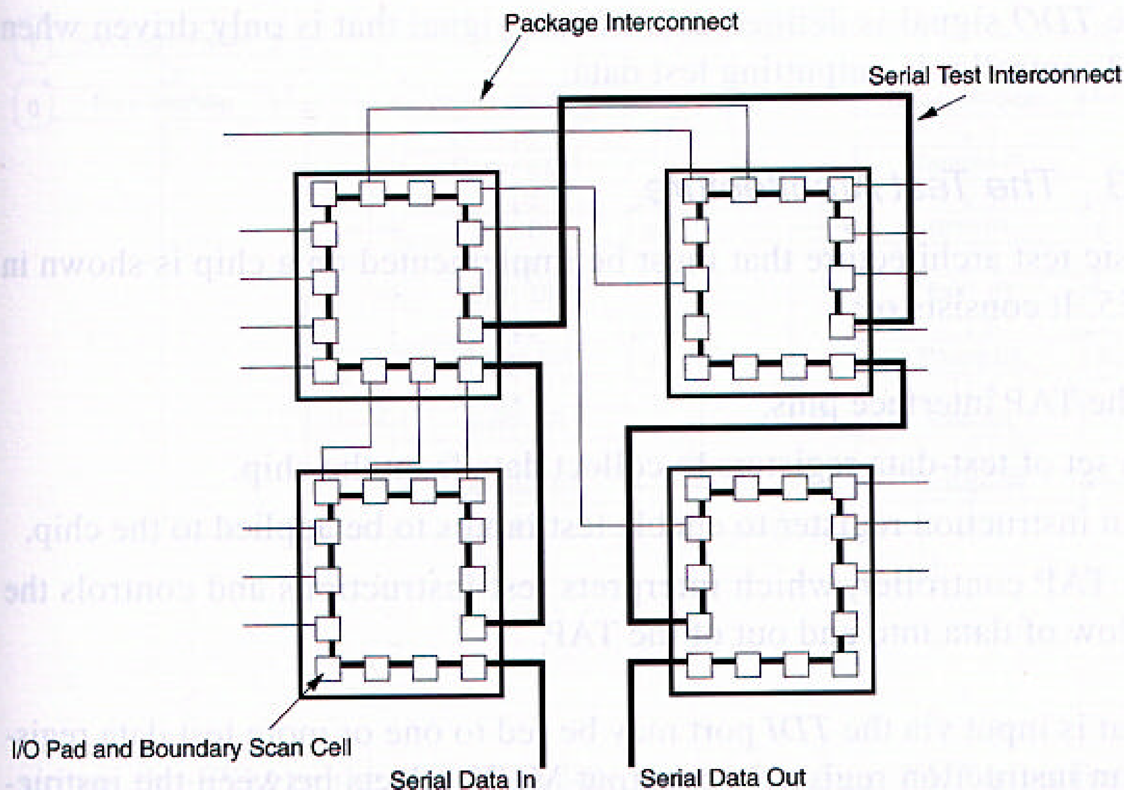


FIGURE 7.24 Boundary scan architecture

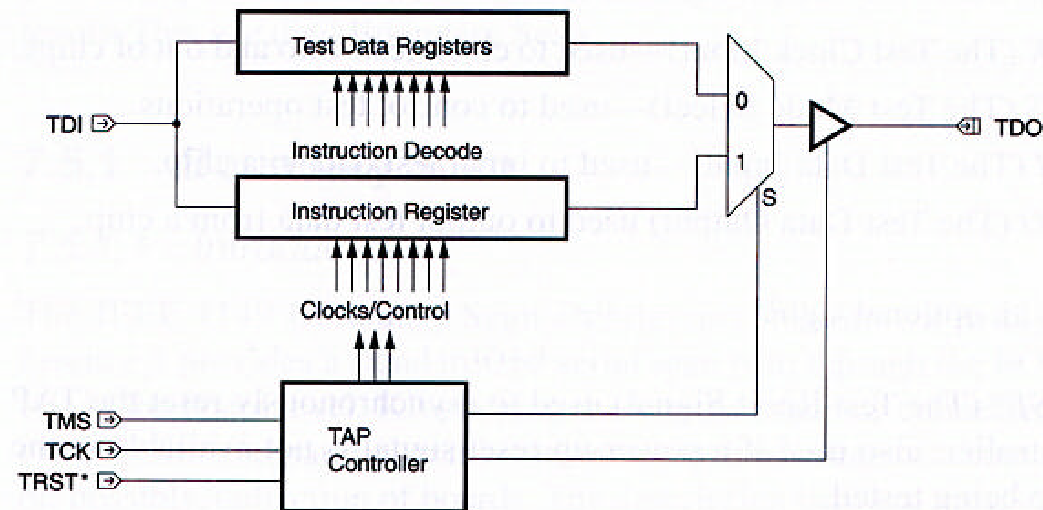


FIGURE 7.25 TAP architecture

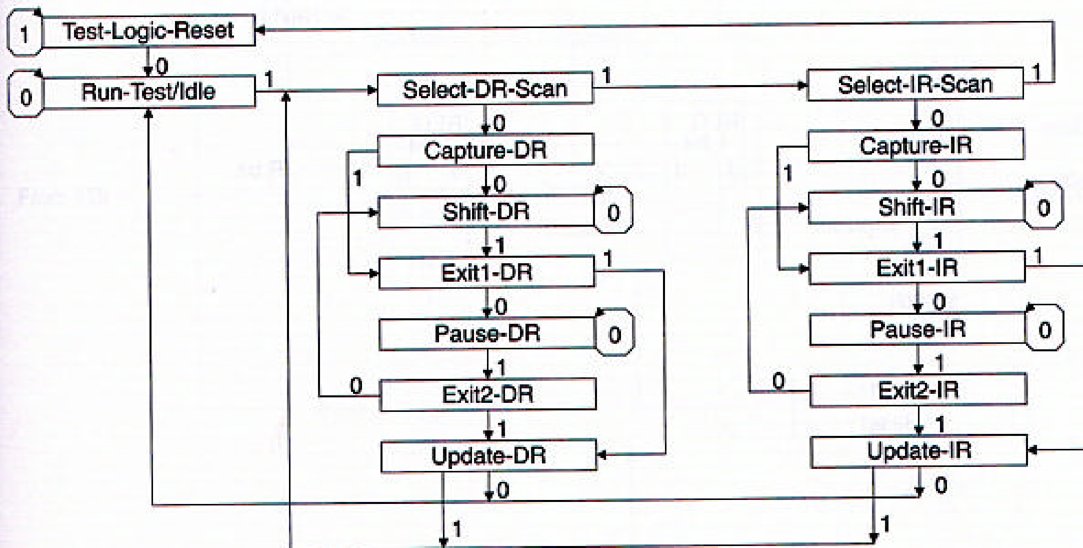
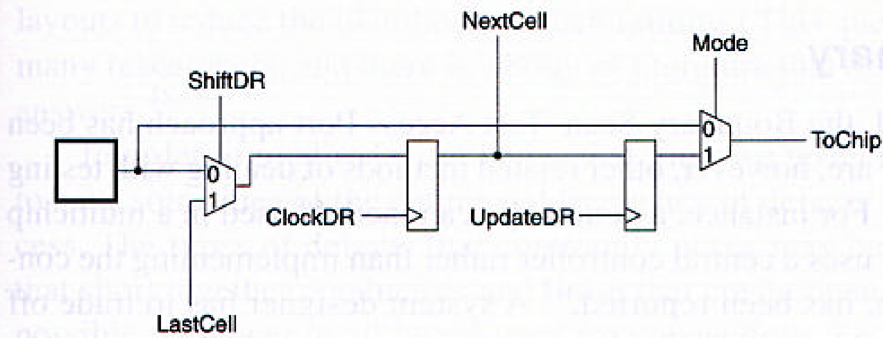


FIGURE 7.26 TAP controller state diagram



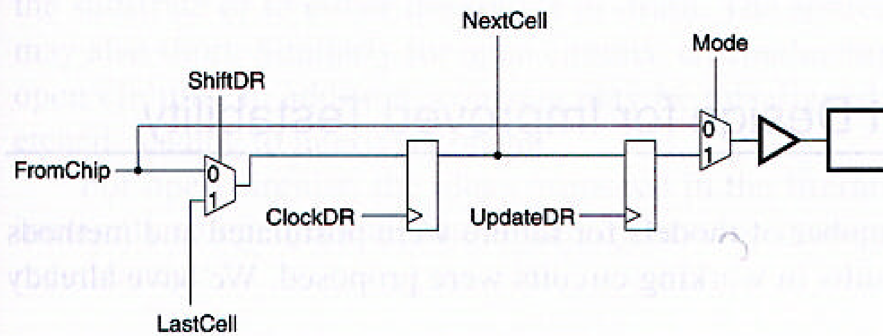


FIGURE 7.29 Boundary scan (a) input and (b) output cells

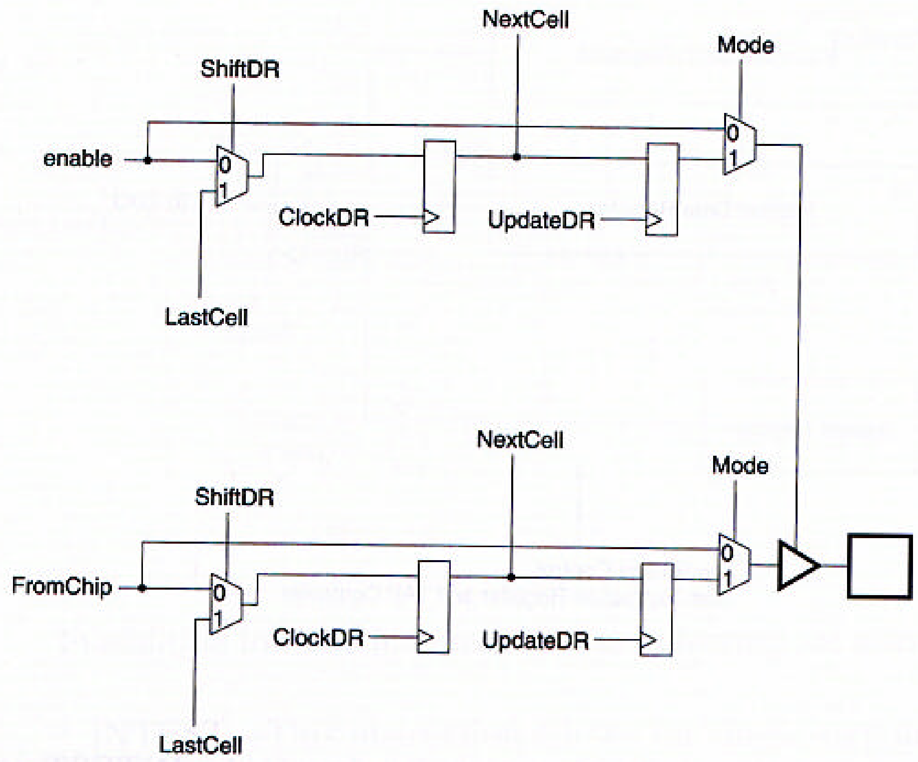


FIGURE 7.30 Boundary scan tristate cell

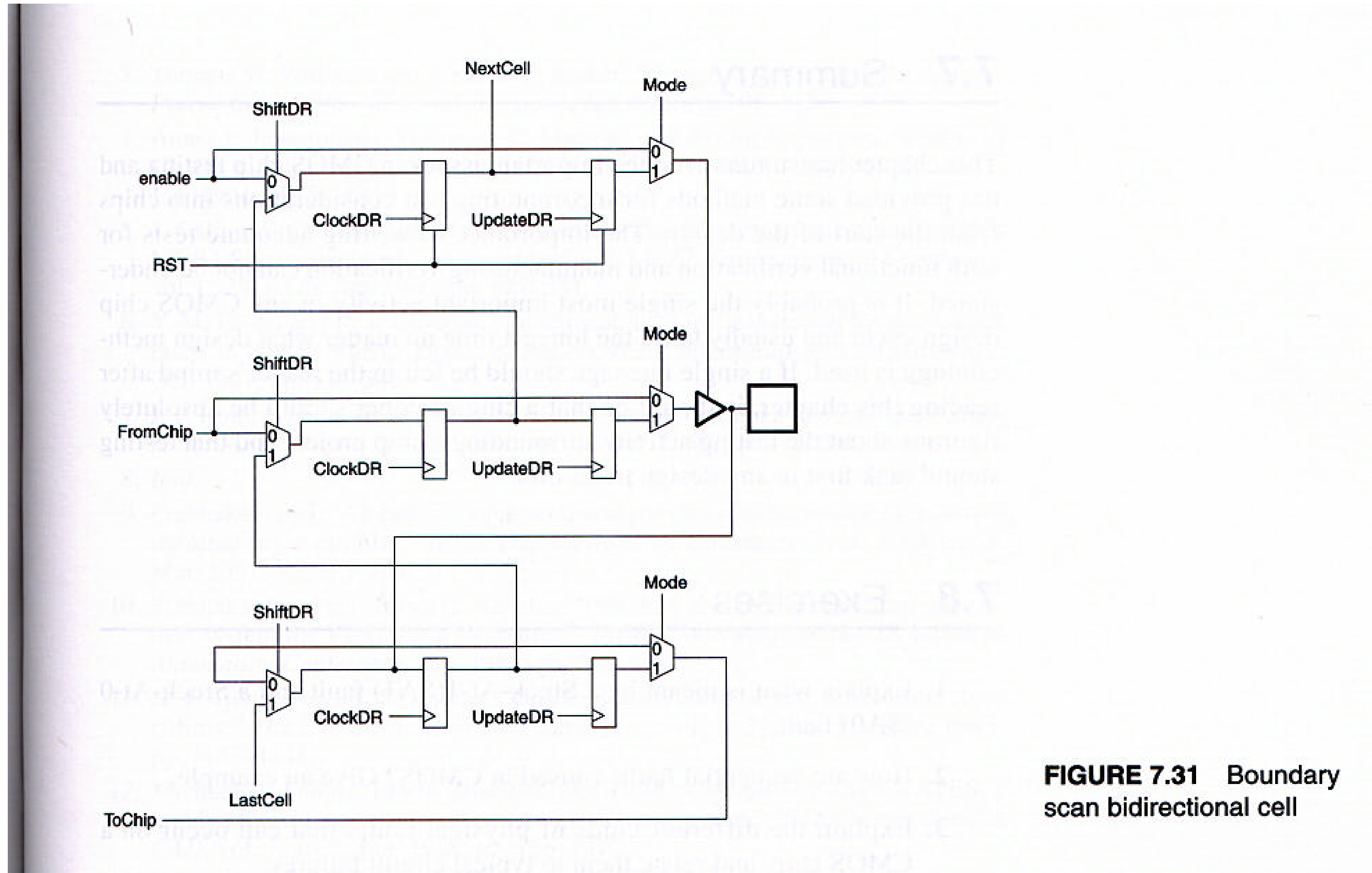


FIGURE 7.31 Boundary scan bidirectional cell