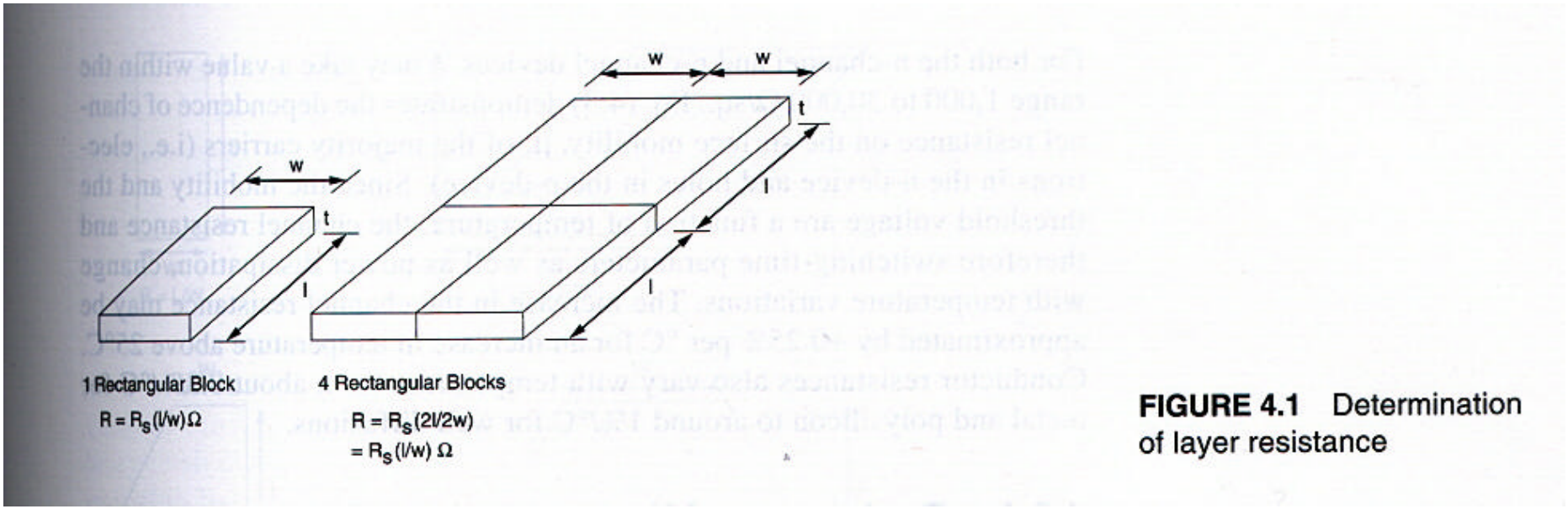

FIGURE 4.1 Determination of layer resistance

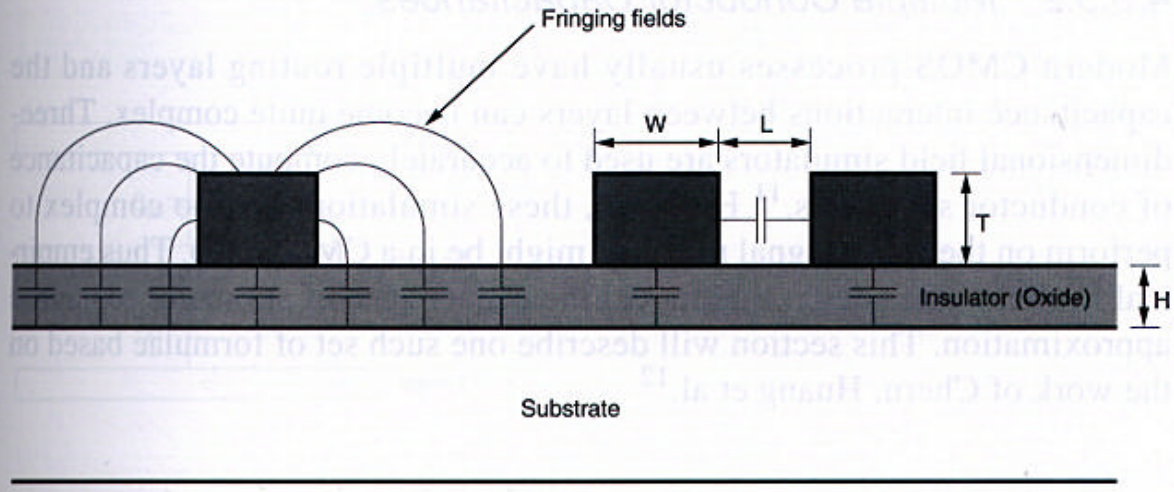

FIGURE 4.9 Effect of fringing fields on capacitance

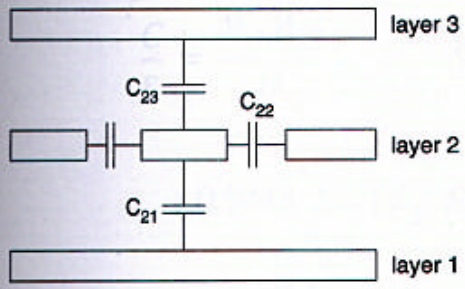

FIGURE 4.12 Specific capacitances in a three-layer-metal system

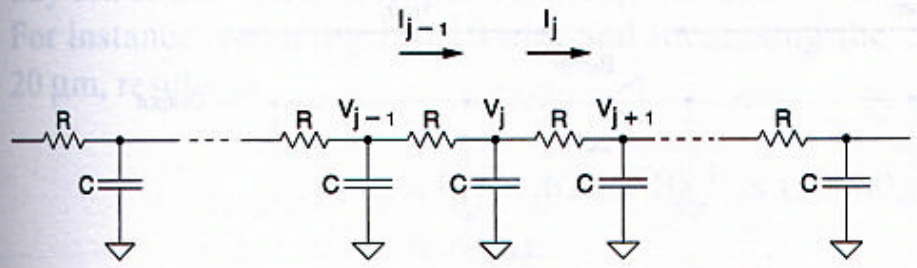

FIGURE 4.15
Representation of long wire in terms of distributed *RC* sections

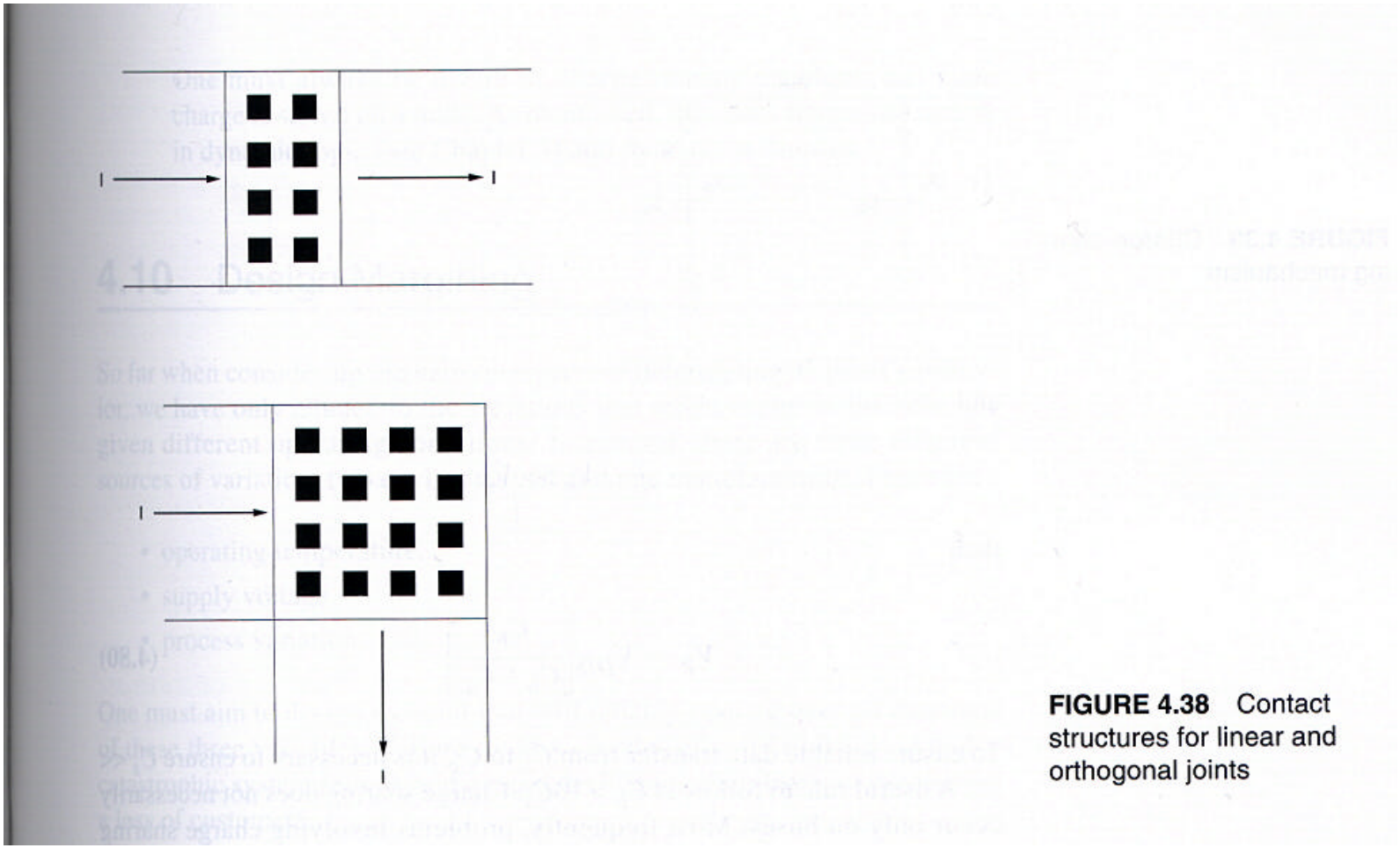

FIGURE 4.38 Contact structures for linear and orthogonal joints

- *Rise time*, t_r = time for a waveform to rise from 10% to 90% of its steady-state value.
- *Fall time*, t_f = time for a waveform to fall from 90% to 10% of its steady-state value.
- *Delay time*, t_d = time difference between input transition (50%) and the 50% output level. (This is the time taken for a logic transition to pass from input to output.)

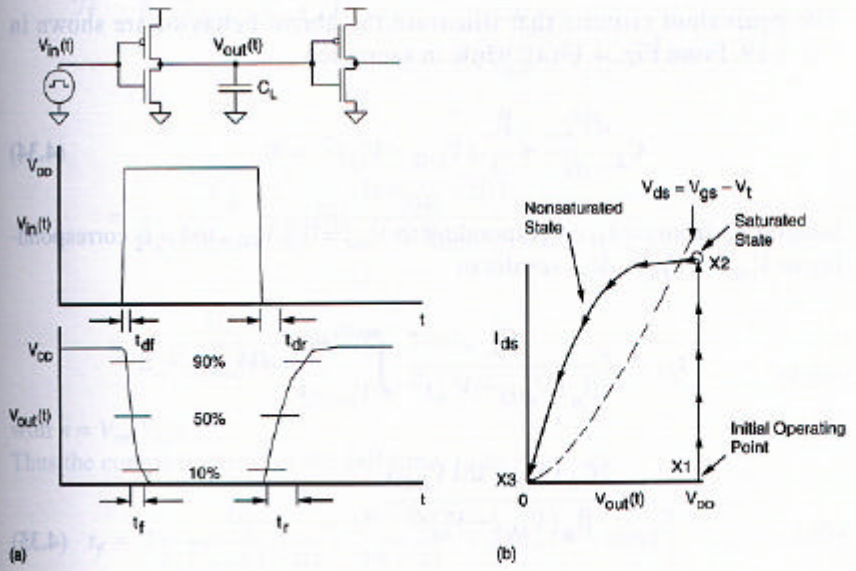

FIGURE 4.18 Switching characteristic for CMOS inverter (a) circuit and waveforms, (b) trajectory of n-transistor operating point during switching

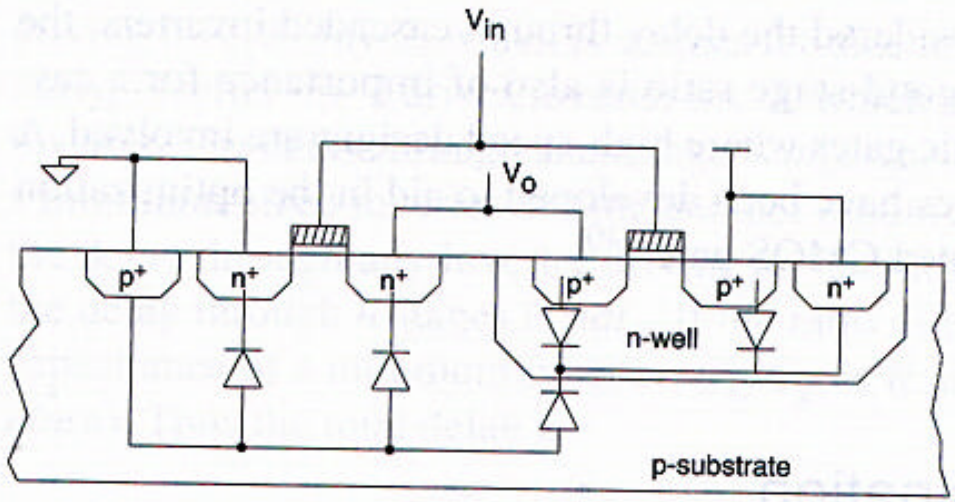

FIGURE 4.35 Model describing parasitic diodes present in a CMOS inverter