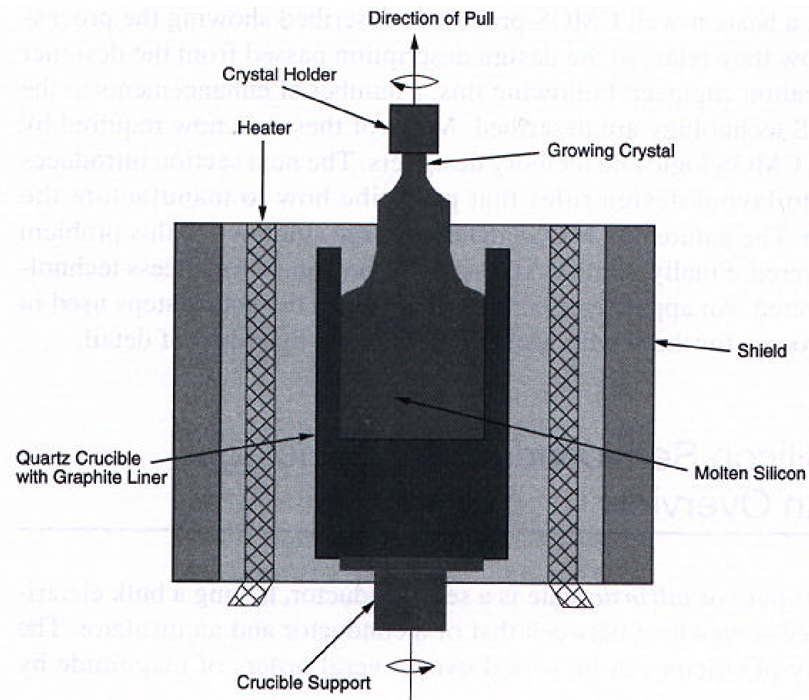


FIGURE 3.1 Czochralski method for manufacturing silicon ingots

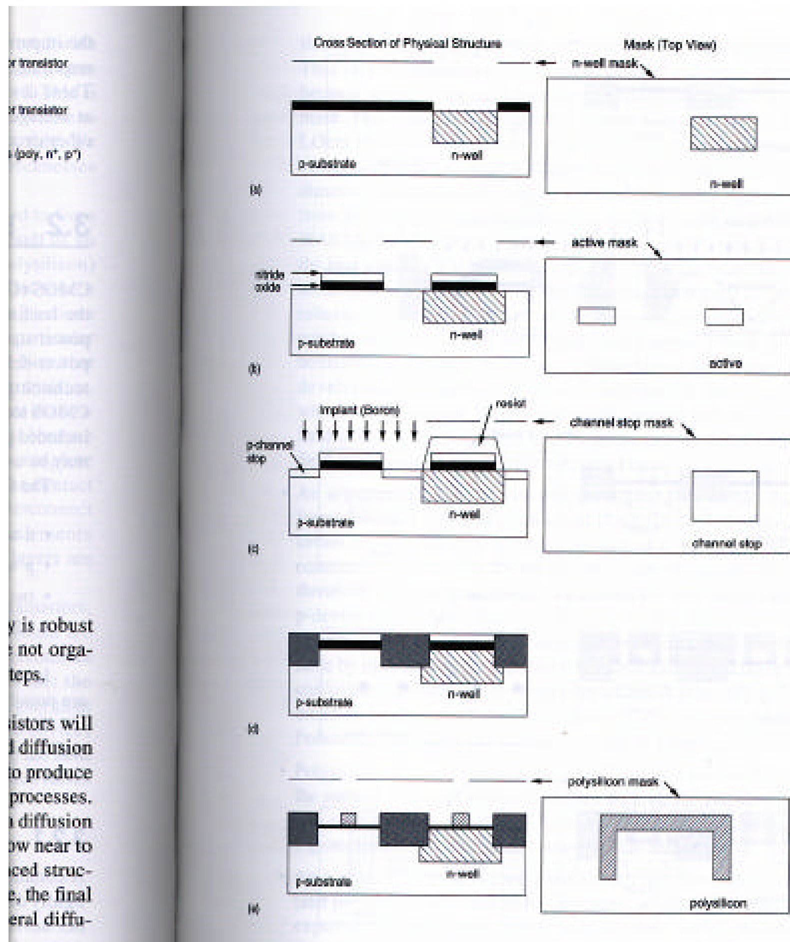


FIGURE 3.7 A typical n-well CMOS process

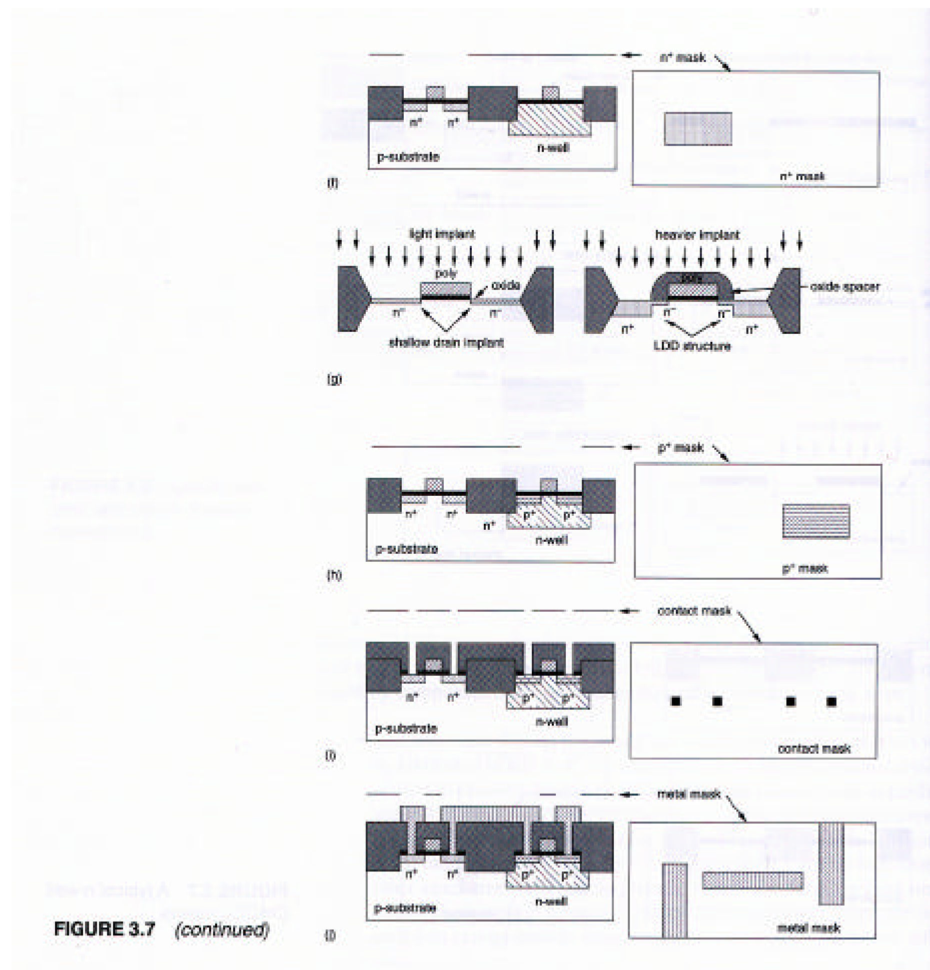
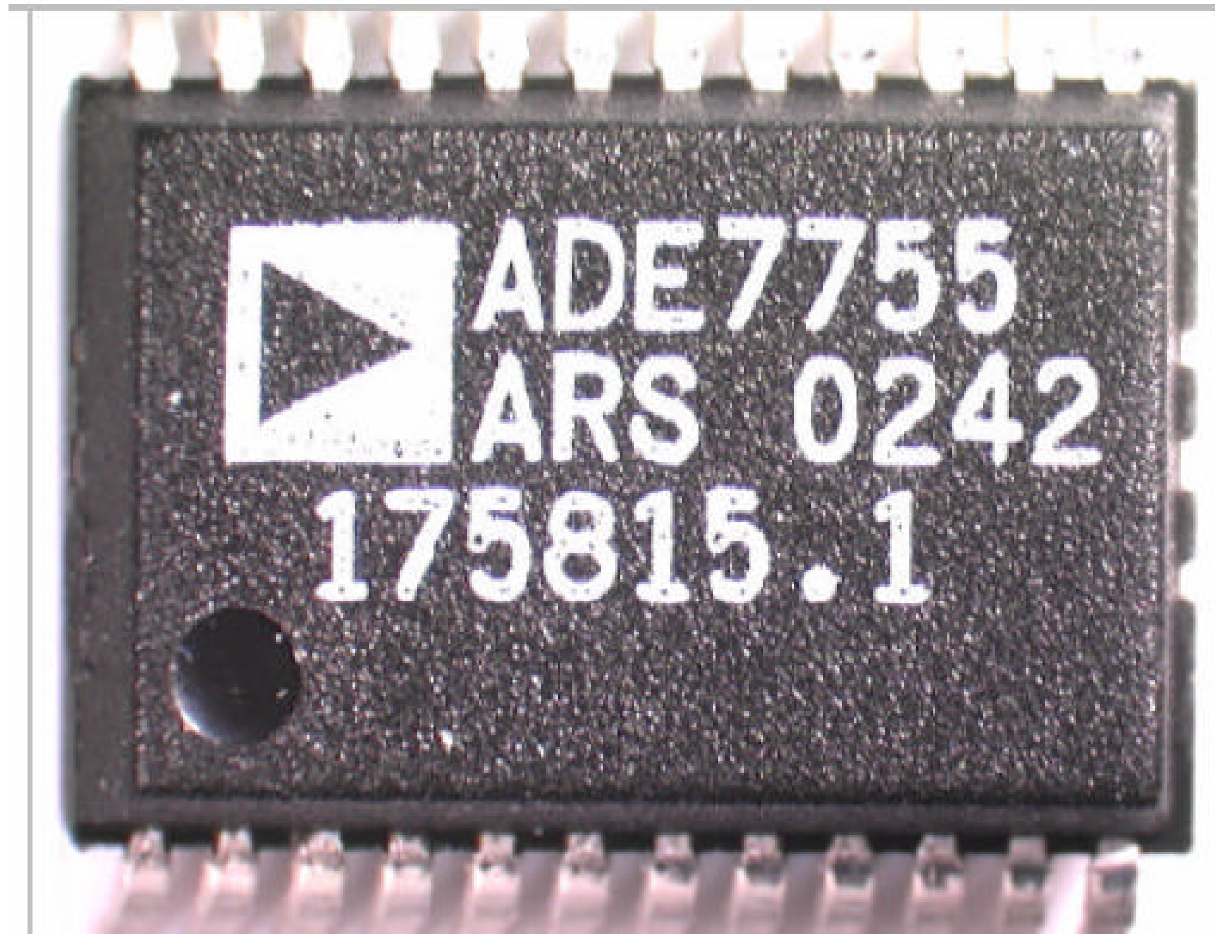
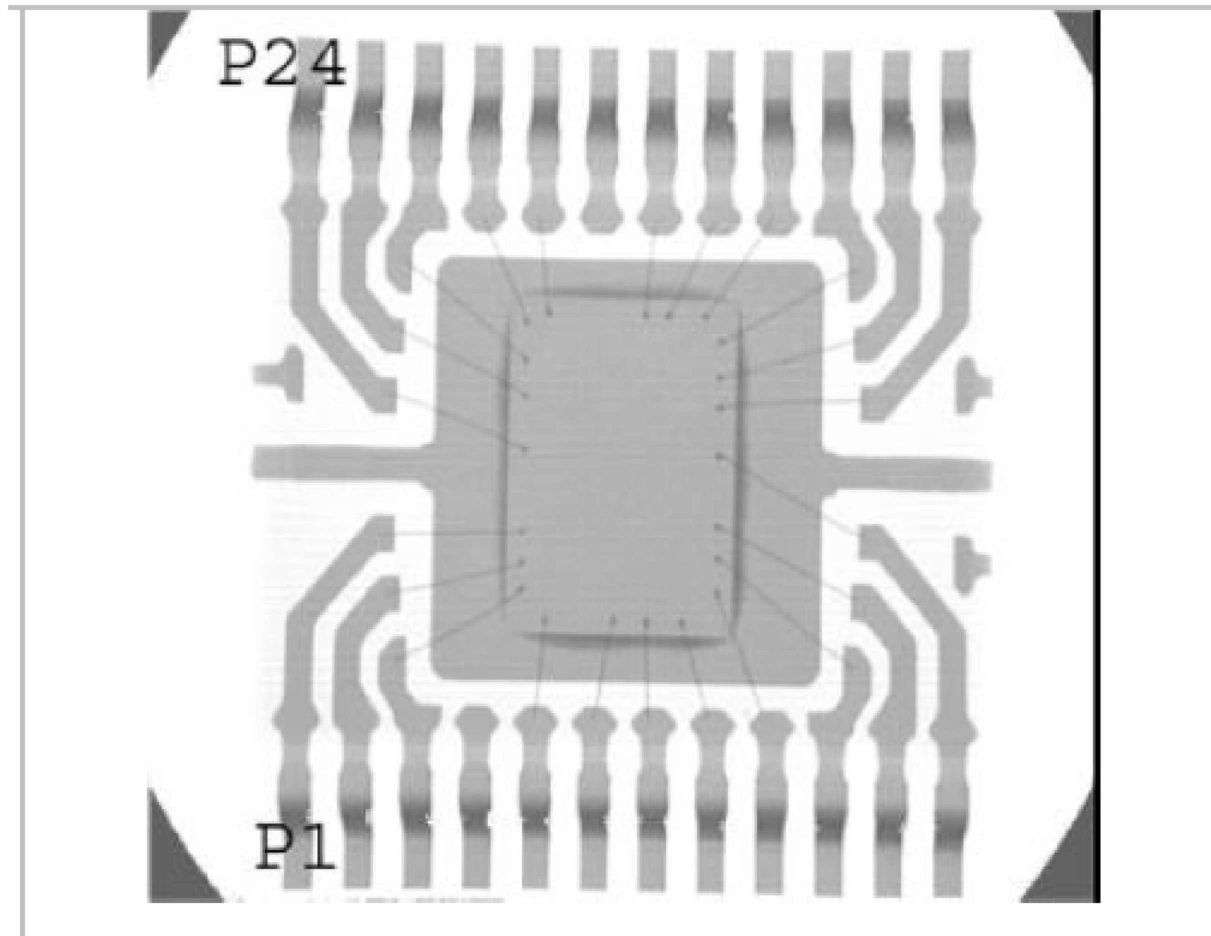
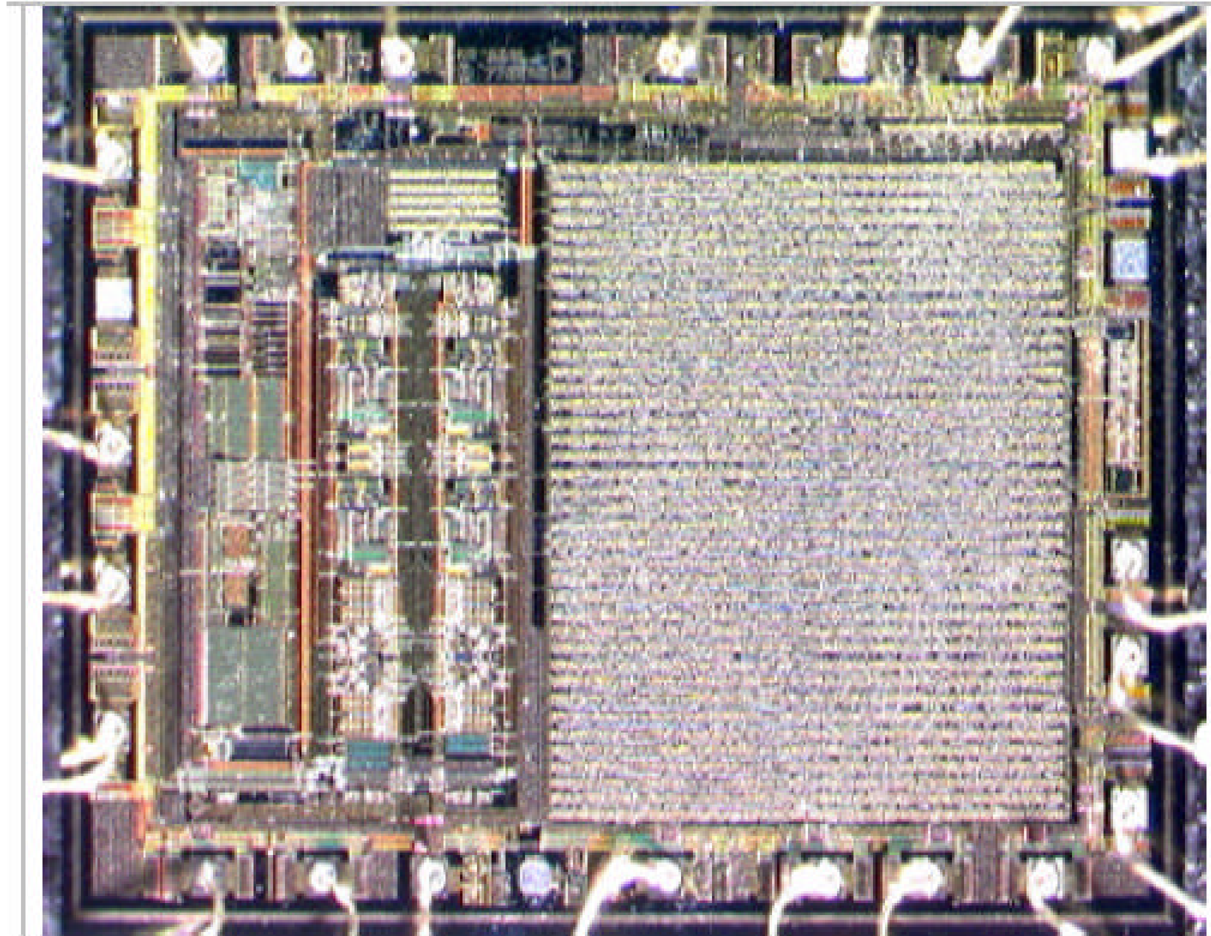
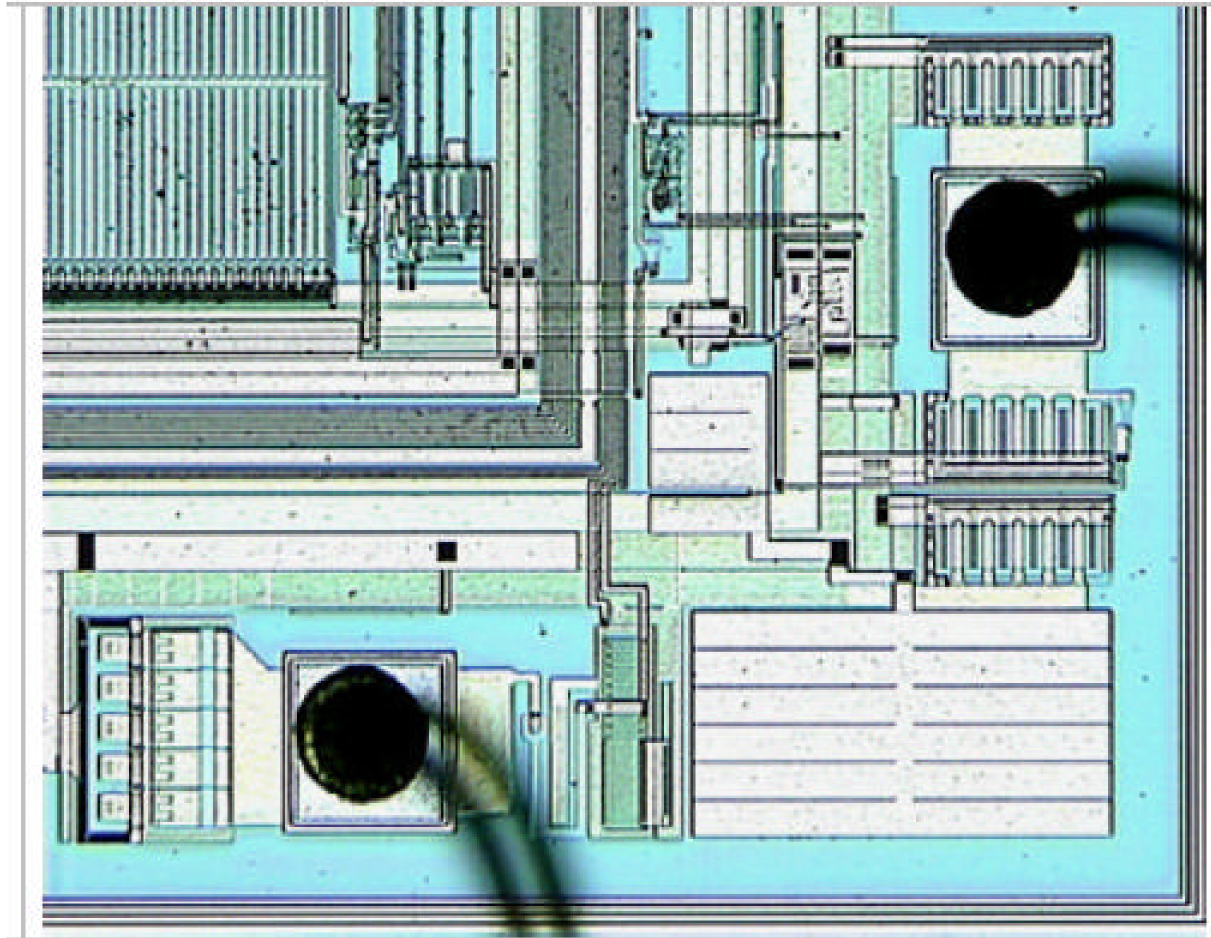


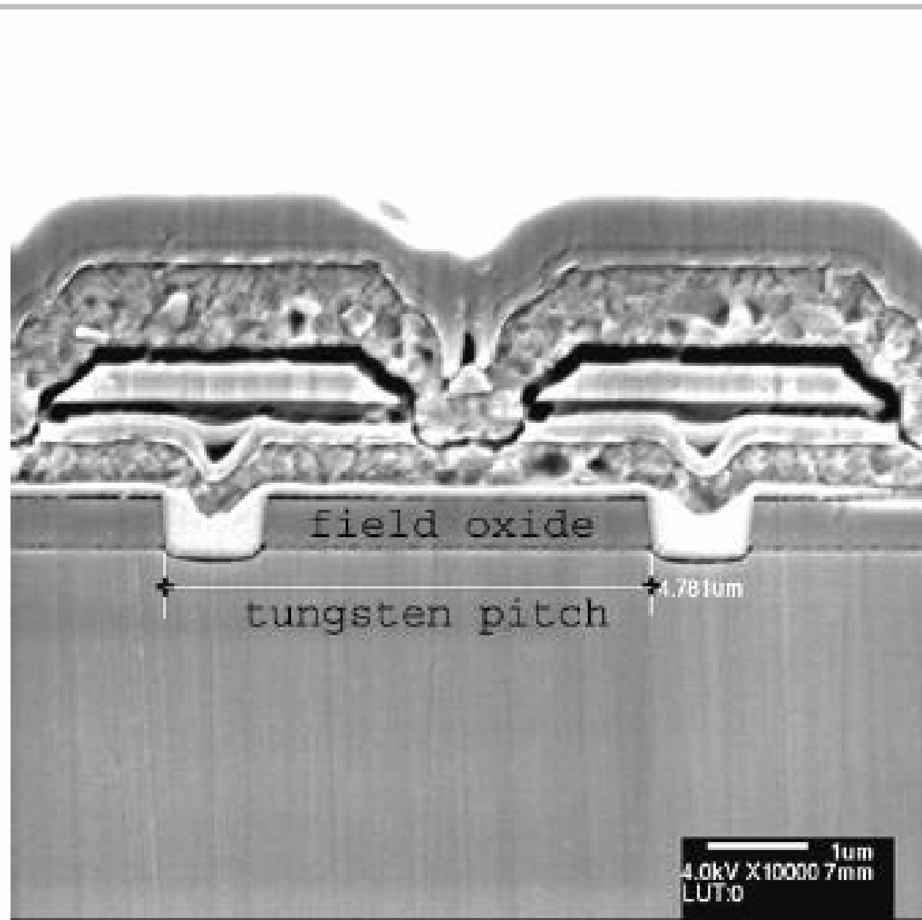
FIGURE 3.7 *(continued)*


ADE7755
ARS 0242
175815.1


P24
P1






field oxide
tungsten pitch
4.781um
1um
4.0kV X10000 7mm
LUT:0

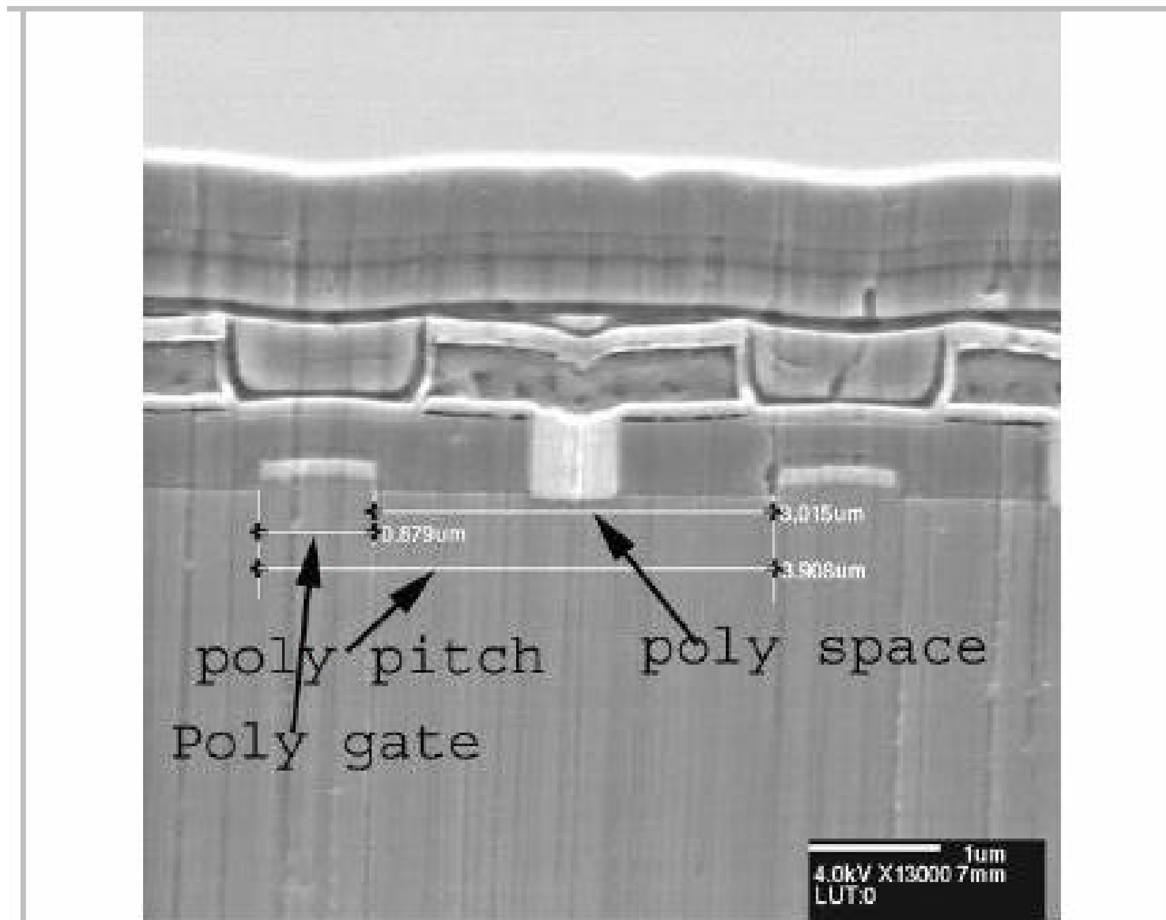

poly pitch
poly space
Poly gate
1um
4.0kV X13000 7mm
LUT:0

TABLE 3.3 Submicron CMOS Process Dimensions

LAYER		NEC[30]	HITACHI[31]	TOSHIBA[32]	HITACHI[33]	IBM[34]
Gate Oxide		15nm	13.5nm	11nm		7nm
Poly1	Width	.55μ (.65μ for p)	.6μ	.5μ	.3μ	.4μ
	Space	.55μ	.6μ	.6μ		
Poly2	Width	.55μ	.6μ	.5μ		
	Space	.55μ	.6μ	.6μ		
Poly3	Width	.55μ	.6μ	.8μ		
	Space	.55μ	.6μ	.7μ		
Poly4	Width		.6μ			
	Space		.6μ			
Contact	Size		.6μ	.6μ		
Metal1	Width	.9μ	.7μ	1.4μ	.3μ	
	Space	.55μ	.6μ	.7μ	.4μ	
Via	Size		.6μ	1.2μ		
Metal2	Width	.9μ	.7μ	1.4μ	.45μ	
	Space	.55μ	.6μ	1.2μ	.65μ	
Metal3	Width				.55μ	
	Space				.75μ	

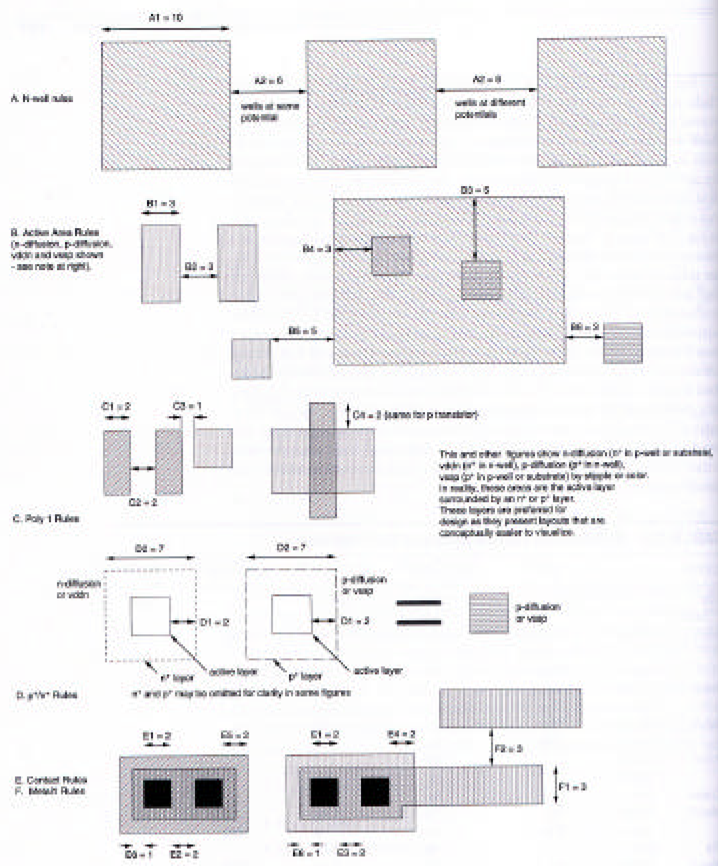


FIGURE 3.25 n-well CMOS design rules

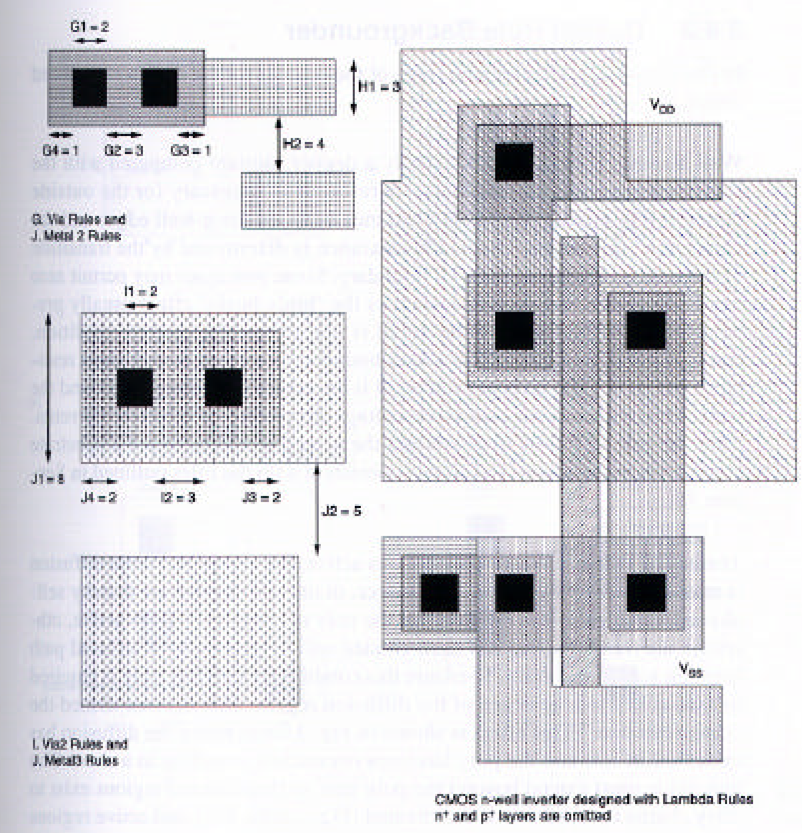


FIGURE 3.25 *(continued)*

The College of New Jersey

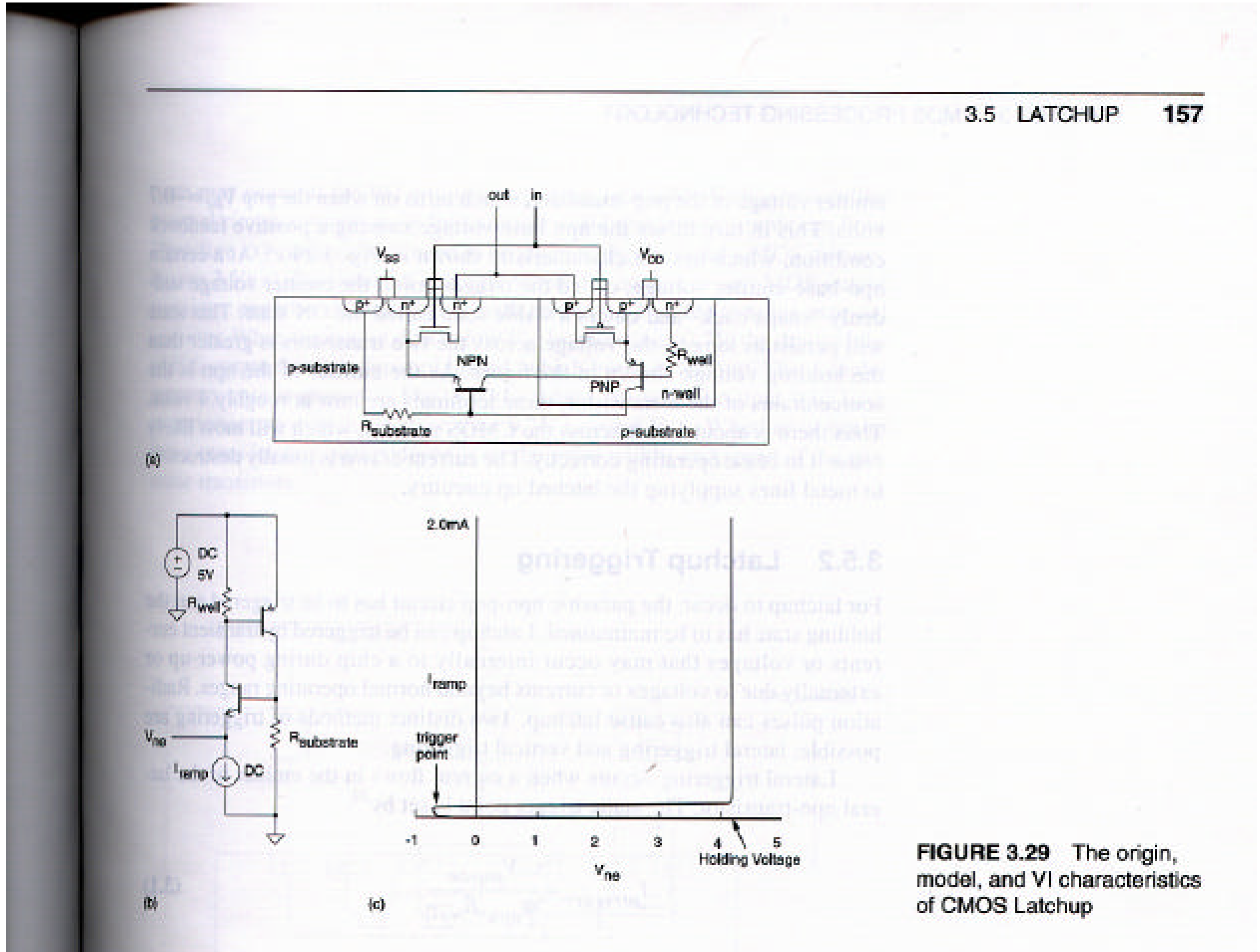


FIGURE 3.29 The origin, model, and VI characteristics of CMOS Latchup

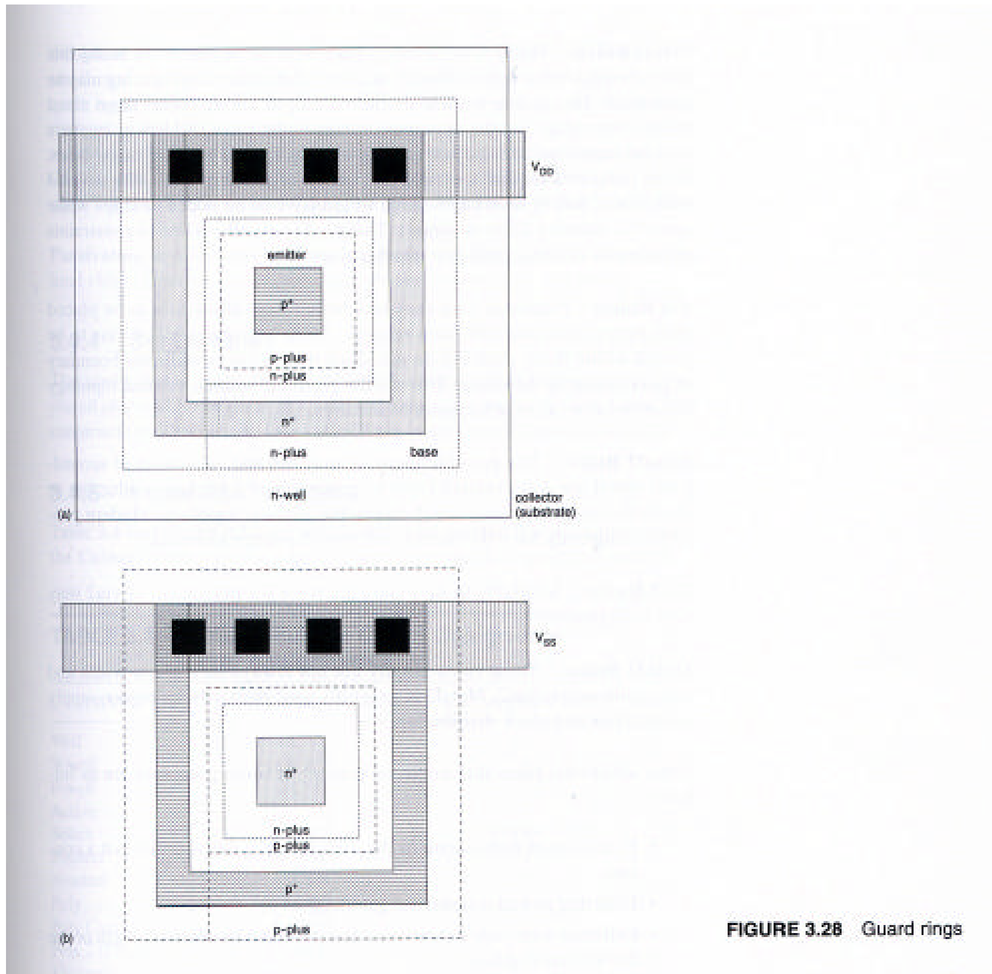


FIGURE 3.28 Guard rings