# ELC 471 - PROJECT #3

# DESIGN OF A PHASE-LOCKED-LOOP

## 1. INTRODUCTION

In this project, a phase-locked-loop (PLL) will be designed. The following figures show examples of the architecture and circuitry of a charge-pump based PLL.

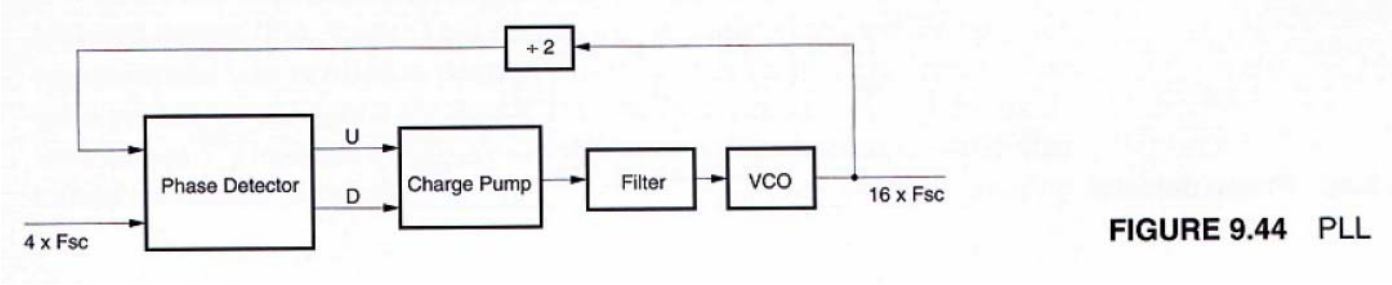


**FIGURE 9.44** PLL

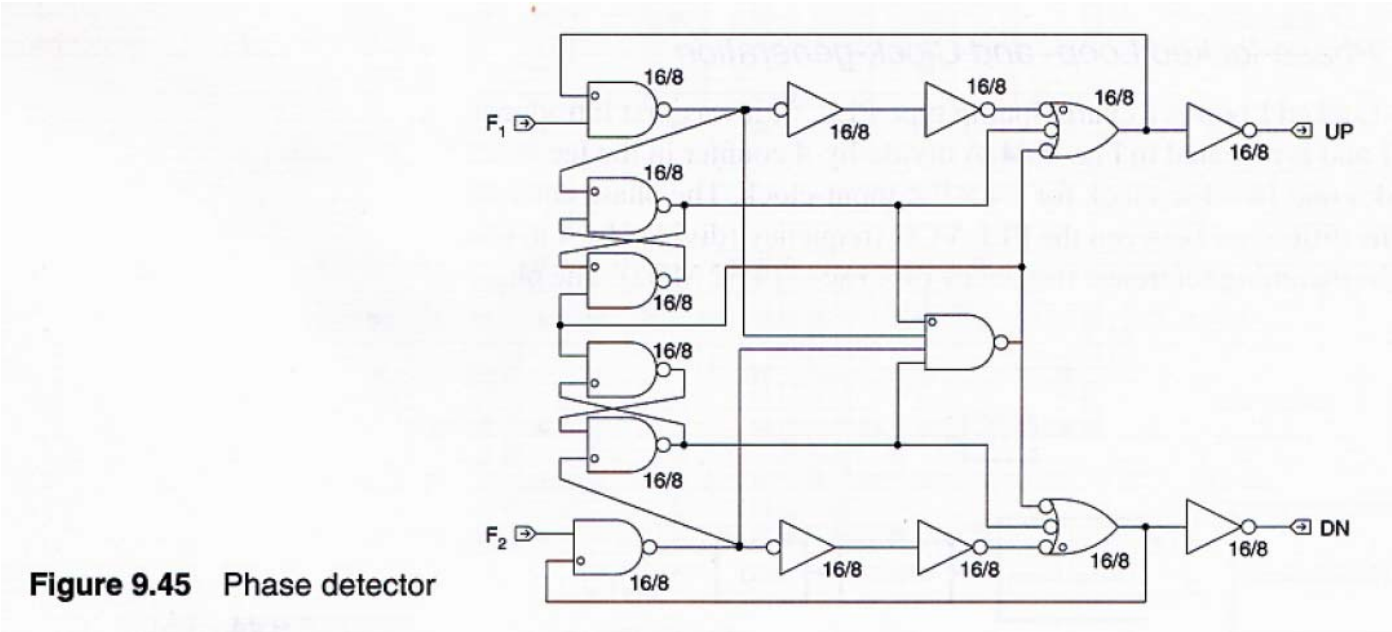


**Figure 9.45** Phase detector

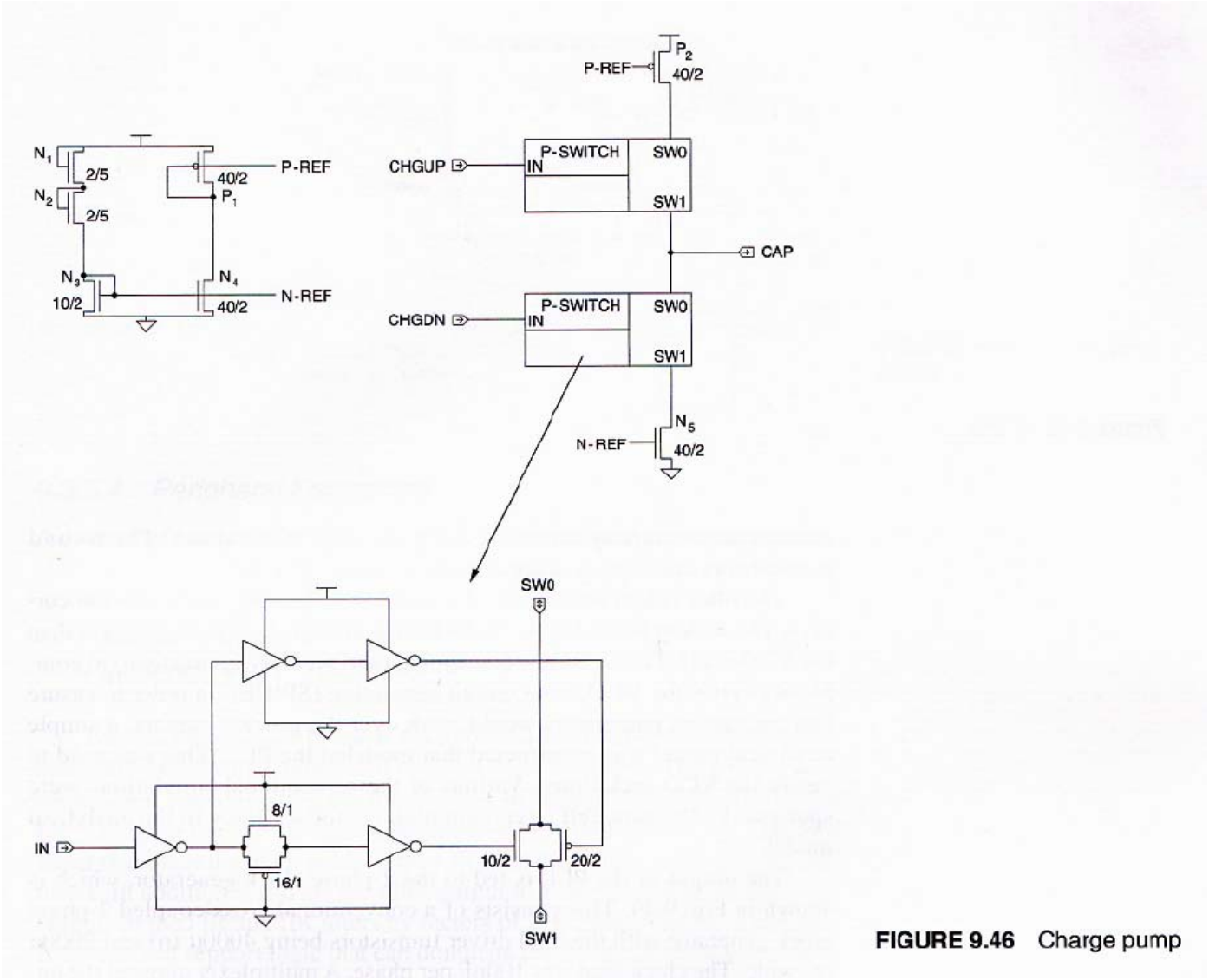


**FIGURE 9.46** Charge pump

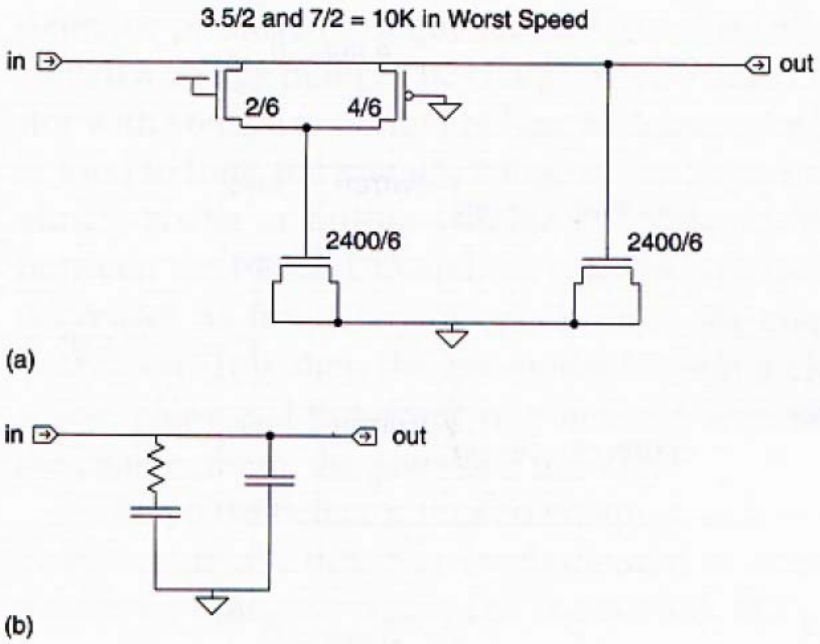


**Figure 9.47** Filter

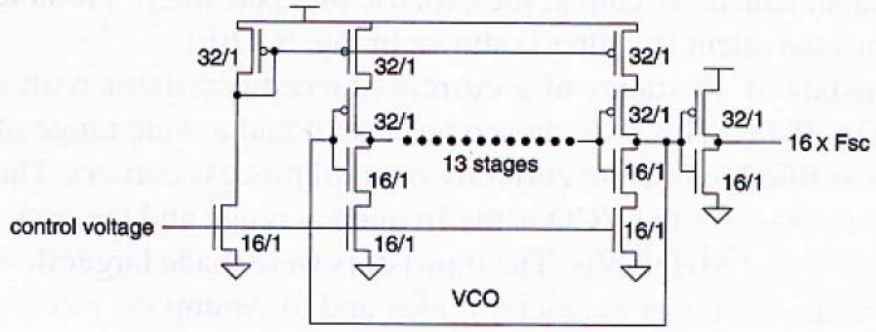


**Figure 9.48** VCO

The first step is for you to choose one of the following functions:

1. Phase Detector design and layout
2. Charge Pump design and layout
3. Filter design and layout
4. VCO design and layout
5. Counter design and layout
6. Top level design and layout

Then there will be two parts to the project. First, the modules will be designed and laid out. Then they will be integrated into a top level to form a PLL based 2X frequency multiplier. A report with, at a minimum, all the items requested to be turned in through these instructions is to be submitted by each student by the due date discussed in class. Each student is expected to do all work individually for his/her module. All reports should be written in a word processor and similar productivity computer tools; no hand written reports will be accepted.

The semiconductor fabrication process that will be used during this project is based on a MOSIS Scalable CMOS process, and it has 3 levels of metal. For this process, $\lambda$ is equal to 0.5 μm, which will make the minimum feature size of $2\lambda = 1.0$ μm. This is what is called a 1 μ process. The nominal $V_{DD}$ is 5V ± 10%, and the junction temperature range is 0 $^{O}$C to 115 $^{O}$C.

In this process, there are six transistor SPICE models available as described subsequently.

Slow (worst performance, lowest power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.7000 KP=2.0000E-5 GAMMA=0.6000 PHI=0.3700 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=2.0000E16)
```

Nominal (typical performance, typical power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.6000 KP=5.0000E-5 GAMMA=0.4000 PHI=0.5550 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=2.0000E16)
```

Fast (best performance, highest power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.5000 KP=8.0000E-5 GAMMA=0.2000 PHI=0.7400 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=2.0000E16)
```

Slow (worst performance, lowest power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.700 KP=0.6250E-5 GAMMA=0.7500 PHI=0.3600 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=4.0000E16)
```

Nominal (typical performance, typical power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.600 KP=1.5625E-5 GAMMA=0.5000 PHI=0.5400 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=4.0000E16)
```

Fast (best performance, highest power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.500 KP=2.5000E-5 GAMMA=0.2500 PHI=0.7200 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=4.0000E16)
```

## 2. DESIGN OF A MODULE

Design your module. Capture the design in SwCAD III, and make sure that it works. Use 0.1 nS input edges where necessary. The SwCAD III simulations should be done with the slowest corner. Make a symbol and a SPICE sub-circuit for the module.

Layout the module, back-annotate the source and drains areas and perimeters, and re-simulate to check that specs are still being met. If not, adjust the design and the layout iteratively, so that the specs are met and the schematic and the layout are coherent.

Include in your report: Schematic of the module. Layout of the module. Waveforms showing that specs are met. Module symbol and sub-circuit.