ELC 471 - PROJECT #2

DESIGN AND CHARACTERIZATION OF A FLIP-FLOP

1. INTRODUCTION

In this project, a flip-flop will be designed and characterized. There will be two parts to the project. First, the flip-fop will be designed and laid out. Then module will be characterized as well. A report with, at a minimum, all the items requested to be turned in through these instructions is to be submitted by each student by the due date discussed in class. Each student is expected to do all work individually. All reports should be written in a word processor and similar productivity computer tools; no hand written reports will be accepted.

The semiconductor fabrication process that will be used during this project is based on a MOSIS Scalable CMOS process, and it has 3 levels of metal. For this process, λ is equal to 0.5 μm, which will make the minimum feature size of 2λ = 1.0 μm. This is what is called a 1 μ process. The nominal V_{DD} is 5V ± 10%, and the junction temperature range is 0 ^{O}C to 115 ^{O}C.

In this process, there are six transistor SPICE models available as described subsequently.

Slow (worst performance, lowest power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.7000 KP=2.0000E-5 GAMMA=0.6000 PHI=0.3700 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=2.0000E16)
```

Nominal (typical performance, typical power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.6000 KP=5.0000E-5 GAMMA=0.4000 PHI=0.5550 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=2.0000E16)
```

Fast (best performance, highest power) NMOS transistor:

```
.model 1UNMOS NMOS(VTO=0.5000 KP=8.0000E-5 GAMMA=0.2000 PHI=0.7400 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=2.0000E16)
```

Slow (worst performance, lowest power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.700 KP=0.6250E-5 GAMMA=0.7500 PHI=0.3600 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=4.0000E16)
```

Nominal (typical performance, typical power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.600 KP=1.5625E-5 GAMMA=0.5000 PHI=0.5400 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=4.0000E16)
```

Fast (best performance, highest power) PMOS transistor:

```
.model 1UPMOS PMOS(VTO=-0.500 KP=2.5000E-5 GAMMA=0.2500 PHI=0.7200 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=4.0000E16)
```

2. DESIGN OF A FLIP-FLOP

Design a D flip-flop that is positive edge triggered, with Q output, and with active low clear input as well. The load to be considered for the design of the flip-flop is 2 SL from Project #1. Design the flip-flop using the same transistor sizes that you used for the standard load in Project #1. This applies to all the transistors in the flip-flop, except for the ones making up the output driver stage. These should be sized per the load discussed above, so that both output rise and fall times are less than 1 nS. Capture the design in SwCAD III, and make sure that it meets the output strength spec. Use 0.1 nS input edges. The additional specs for this flip-flop is that the hold time is 0 nS or negative and we will take whatever setup time we get. The SwCAD III simulations should be done with the slowest corner for the output strength and the fastest corner for the hold time. Make a symbol and a SPICE sub-circuit for this flip-flop.

Layout the flip-flop, back-annotate the source and drains areas and perimeters, and re-simulate to check that specs are still being met. If not, adjust the design and the layout iteratively, so that the specs are met and the schematic and the layout are coherent.

Include in your report: Had calculations for load capacitance and output driver transistors sizes. Schematic of the flip-flop. Layout of the flip-flop. Waveforms showing that specs are met. Flip-flop symbol and sub-circuit.

3. CHARACTERIZATION OF A FLIP-FLOP

At this point, there is a fully designed and laid out circuit that meets both functional and performance requirements. Then the flip-flop must be characterized.

Characterize the following parameters: t_{CQLH}, t_{CQHL}, t_{SU}, rise and fall times of the output, and t_{RQ}. The characterization is to be done at this process, voltage, and temperature (PVT) corner with all the combinations of the following loads and slews:

- Slow corner: slow n-channel SPICE model, slow p-channel SPICE model, low voltage, and high temperature.
- Loads: 2 SL, 8 SL
- Slews (10% to 90%): 0.2 nS, 4nS

These characterization will yield one 2 x 2 table for each of the parameters.

Characterize the following parameter: t_{HO}. The characterization is to be done at this process, voltage, and temperature (PVT) corner with all the combinations of the following loads and slews:

- Fast corner: fast n-channel SPICE model, fast p-channel SPICE model, high voltage, and low temperature.
- Loads: 2 SL, 8 SL
- Slews (10% to 90%): 0.2 nS, 4nS

These characterization will yield one 2 x 2 table for each of the parameters.

Include in your report: characterization tables, and SwCAD III simulation results of the supply current for two cycles of operation with all nominal transistors parameters, 5V V_{DD}, 25 ^{O}C, 2 nS 10-90% input slews, and 4 SL at the output.