ELC 471 - PROJECT #1

DESIGN OF A COMPLEX GATE

1. INTRODUCTION

In this project, a complex gate will be designed. There will be three parts to the project. First, a standard load (SL) will be designed. The next step will be the design of the complex gate, then the layout. A report with, at a minimum, all the items requested to be turned in throughout these instructions is to be submitted by each student by the due date informed during class. Each student is expected to do all work individually. All reports should be written in a word processor and similar productivity computer tools; no hand written reports will be accepted.

The semiconductor fabrication process that will be used during this project is based on a MOSIS Scalable CMOS process, and it has 3 levels of metal. For this process, λ is equal to 0.5 μm, which will make the minimum feature size of 2λ = 1.0 μm. This is what is called a 1 μ process. The nominal V_{DD} is 5V ± 10%, and the junction temperature range is 0 ^{O}C to 115 ^{O}C.

In this process, there are six transistor SPICE models available as described subsequently.

Slow (worst performance, lowest power) NMOS transistor:

```
.model S1UNMOS NMOS(VTO=0.7000 KP=2.0000E-5 GAMMA=0.6000 PHI=0.3700 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=2.0000E16)
```

Nominal (typical performance, typical power) NMOS transistor:

```
.model N1UNMOS NMOS(VTO=0.6000 KP=5.0000E-5 GAMMA=0.4000 PHI=0.5550 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=2.0000E16)
```

Fast (best performance, highest power) NMOS transistor:

```
.model F1UNMOS NMOS(VTO=0.5000 KP=8.0000E-5 GAMMA=0.2000 PHI=0.7400 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=2.0000E16)
```

Slow (worst performance, lowest power) PMOS transistor:

```
.model S1UPMOS PMOS(VTO=-0.700 KP=0.6250E-5 GAMMA=0.7500 PHI=0.3600 LAMBDA=0.0100
+LD=0.1000E-6 TOX=2.0000E-8 NSUB=4.0000E16)
```

Nominal (typical performance, typical power) PMOS transistor:

```
.model N1UPMOS PMOS(VTO=-0.600 KP=1.5625E-5 GAMMA=0.5000 PHI=0.5400 LAMBDA=0.0100
+LD=0.0500E-6 TOX=1.5000E-8 NSUB=4.0000E16)
```

Fast (best performance, highest power) PMOS transistor:

```
.model F1UPMOS PMOS(VTO=-0.500 KP=2.5000E-5 GAMMA=0.2500 PHI=0.7200 LAMBDA=0.0100
+LD=0.0100E-6 TOX=1.0000E-8 NSUB=4.0000E16)
```

2. DESIGN OF A STANDARD LOAD

Design an inverter that will be used as standard load in a characterization procedure in Project #2. This inverter shall utilize a minimum size n-transistor, and the appropriate minimum size p-transistor to achieve within 10% equal rise and fall times and/or propagation delays without any load and using the slow transistors parameters. First, layout an n and a p transistor in Magic to find out what are the minimum transistor sizes. Capture and simulate the inverter in SwCAD III with 0.1 nS input edges. Then, calculate the input capacitance of the inverter.

Make a symbol and a SPICE sub-circuit for this inverter.

Magic tips:

- When Magic comes up, type ":source magic".
- The minimum grid spacing ("grid" command) represents 1 λ.

Include in your report: Layout of the minimum p and n transistors in Magic, 1st order design calculations, SwCAD III schematic, simulations results for one input cycle with input and output signals in the same plot pane, input capacitance calculations, inverter symbol, and inverter SPICE sub-circuit.

3. DESIGN OF A COMPLEX GATE

Design and simulate in SwCAD III a logic gate to perform the following function:

$$f = \overline{A\,(B + C\,D\,E)}$$

Performance requirements of this gate are:

- This gate shall employ minimum effective size transistors as defined by the transistor sizes of the inverter designed previously in this project.

To get the design done, simulate with 0.1 nS input edges, and use slow transistor parameters for all simulations in this part.

Include in your report: SwCAD III schematic and functional simulation results with one signal per plot pane.

4. LAYOUT OF A COMPLEX GATE

Layout the complex gate in Magic as compactly and as square as possible.

Include in your report: final layout from Magic.